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SENSOR DATA CORRELATION SYSTEM DEVELOPMENT (DESIGN PHASE).(U)
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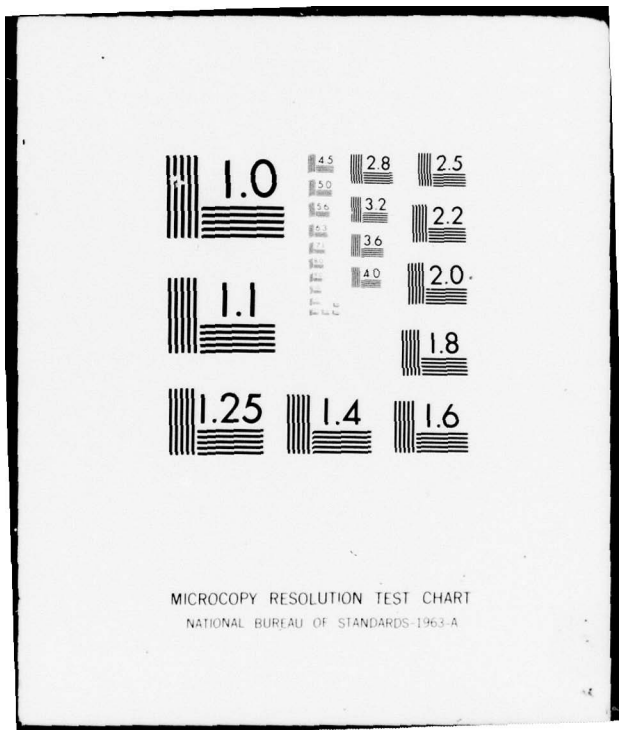
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RADC-TR-77-191
Final Technical Report
June 1977

SENSOR DATA CORRELATION SYSTEM DEVELOPMENT (DESIGN PHASE)

Sanders Associates

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ROME AIR DEVELOPMENT CENTER
Air Force Systems Command
Griffiss Air Force Base, New York 13441

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This report has been reviewed and is approved for publication.

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Message Processing
Sensor Data Correlation

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The design of an Associative/Parallel (A/P) File and Processor for handling large intelligence data bases is described. A System overview presents the major hardware and software components of the system and a functional description presents system capabilities from a user's point of view. A description of the general system data flow is given, and major components of the A/P File and Processor are described in detail, including a specification for the disk file and a parts breakdown for the processor. Preliminary schedule, plan and cost estimate for fabricating and testing one complete

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system are given. The report also includes a system specification and preliminary acceptance test plan.

TABLE OF CONTENTS

TABLE OF CONTENTS CONT.

TABLE OF CONTENTS CONT.

TABLE OF CONTENTS CONT.

TABLE OF CONTENTS CONT.

LIST OF ILLUSTRATIONS

LIST OF TABLES

EVALUATION

The significance of this contractual effort is that it provides design specifications for a unique data processing configuration based upon utilization of an associative/parallel processor. The technology incorporated in this configuration permits rapid search and retrieval of unindexed data, both numeric and non-numeric, using flexible search criteria. The operator of the system is able to interact with it through an input/output CRT terminal. Input data can be obtained from a large random access storage device or from communications lines, and can be handled at a maximum 4 Megabyte per second rate. The system has applications in searching large data bases, filtering an input data stream and searching input messages in real time.

It is planned to fabricate a system based on the design specified in this report, and provide this pilot system to support Air Force Indications and Warning functions.

This effort supports technical program objective R3B by providing an advanced automated intelligence data handling capability.

JOHN V. WEBER
Project Engineer

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SECTION 1

INTRODUCTION AND SUMMARY

1.1 Introduction

The detailed design of the standalone version of the Sensor Data Correlation System is complete. The system includes the SCAT 16 Associative Processor, a controller for the CDC 9790 Disk Storage Unit, and a high speed parallel bus interface to the PDP-11/45 system host computer. The design also includes applications software module designs for handling teletype messages with provisions for additional modules for handling intermixed fixed format records having a wide range of data formats and record size.

The SCAT (Standalone Content Addressable Terminal) processing concept was developed in 1974 as an outgrowth of the Sanders OMEN family of orthogonal memory design, covered by U.S. Patent 3,277,449. This memory architecture permits serial external data transfers with the host and at the same time parallel internal data transfers for associative/parallel processing. The OMEN processors contained parallel vertical arithmetic units for high-speed, bit-serial processing of numeric data. Their design was optimized for high speed matrix manipulations for digital signal processing particularly for performing fast Fourier transforms. The OMEN systems did not include a high speed parallel transfer mass storage system.

The SCAT/32 design, described in Sanders proposal WAZDC, 6 January 1975, employed an 8-track parallel, 25M byte fixed head disk, a 32 channel orthogonal memory, and a simplified vertical arithmetic unit optimized for fast associative search and retrieval of fixed format records stored on the disk.

The present SCAT 16 design, described herein employs up to 4, 4-track parallel, 300 M byte moving head disks, a 16 channel orthogonal memory, and a vertical arithmetic unit expanded for handling text as well as fixed format records. The system can be expanded to handle 8/16-track parallel disks to increase throughput, a larger number of search keys to provide faster response to multiple queries, and wider textword windows to accommodate longer search phrases. However, the system as currently designed will handle all of the data bases described in proposal WAZDC as well as providing high performance/cost for sensor data correlation.

Section 2 of this report presents a general equipment description, an overview of system operations and capabilities, subsystem specifications, a functional description of the software, system data flow, a detailed description of the Associative Processor, and a detailed description of the operator interface.

Section 3 presents a detailed itemization of system hardware, identifies long lead items with their lead times, and includes a piece part breakdown of the Associative Processor.

Section 4 presents a detailed plan for the development of a pilot model of the system in the standalone configuration together with schedule and cost estimate.

Section 5 presents a system functional specification and a preliminary test plan for testing the system.

Appendix A presents a detailed functional specification of the SCAT applications software for the initial system.

1.2 Executive Summary

The Sensor Data Correlation System (SDCS) has been designed as a general purpose data storage and retrieval system for intelligence data handling applications. Although specified for handling the NMIC 5-day message file using simple associative search techniques, the capabilities of the SDCS, as presently designed, far exceeds this requirement. For a number of years there has been an outstanding requirement for a low cost Associative/Parallel (A/P) processor which could handle non-numeric as well as numeric data and which, using associative search techniques, would greatly decrease data retrieval times while eliminating the need for complex file directories. The SDCS fulfills this need.

The SDCS includes a large (up to a gigabyte) disk file and A/P processor. Together, these can be attached as an intelligent mass memory peripheral to a non-dedicated PDP-11, or similar, host. As a result, the capabilities of the host system are greatly enhanced by the addition of a large content addressable file whose records can be rapidly searched and specified data accurately retrieved. Because the A/P File and Processor is intelligent, it imposes a minimal CPU load on the host. An intelligent graphics terminal can also be added to provide interactive control of the system.

The SDCS can also be provided in a standalone configuration with a PDP-11/45 host, one or more A/P File and Processors, and one or more interactive terminals. In either configuration the large disk File serves as a temporary or semi-permanent repository of fixed format and/or free format records or documents which may be readily and accurately retrieved on the basis of specific content. Examples of records which may be retrieved using the associative search technique are teletype messages, technical documents, and sensor reports. Search algorithms (i.e., queries) are composed on the CRT terminal and transferred to the A/P File and Processor for immediate execution or filing for later use. In a multiuser environment filed queries may serve as dissemination profiles which are immediately recalled for serial execution as new records are input.

Accompanying each query is a retrieval algorithm (i.e., desired response) which specifies whether all or selected portions of hit records are to be retrieved for display or further processing. Data is retrieved on-the-fly as soon as a hit is scored whenever the content of the record matches that specified by the query. When a file search is initiated, record data is continuously transferred from the parallel track disk to the A/P Processor for examination and the on-the-fly hit retrieval permits this rapid transfer to continue uninterrupted until the file is exhausted.

The system is designed to provide not only a very rapid search and retrieval capability but a highly accurate one as well. For example, the query can specify that numerical attributes be exactly equal to the key value or fall within or outside of specified limits. Words in text may be required to exactly match or to partially match the keywords in the query. Groups of textwords, or their synonyms, may be required to occur or not occur within a given proximity and/or order. A soft match may also be specified wherein a minimum number of keywords from a list must match.

Using a between limits search the system can be used for the rapid plotting of histograms for analyzing the statistics of selected record attributes. For sensor data correlation the system can be used to screen and selectively file an input data stream of sensor reports. The file can be searched at any time to extract for display position coordinates and other data for targets of interest on a detailed map underlay selected from a map library also stored on the disk. By this means target reports from different sensors at different times may be rapidly correlated using time compression display techniques. Although the system will support very sophisticated queries with complex search algorithms, it has been designed with the

untrained operator in mind. Special function keys, cues, menus, and feedback permit the novice to employ as much or as little of the power of the machine as he desires.

SECTION 2
SYSTEM DESIGN

This section describes the overall SDCS in both a standalone configuration and in a configuration where the major SCAT components are integrated into an existing or planned I&W computer network. This description is followed by an overview of system operation for retrospective search, sensor data correlation, and data stream monitoring. Next, a detailed description of the SCAT Associative/Parallel (A/P) processor is given followed by a description of the SCAT software and data flow within the system.

2.1 General

The Sensor Data Correlation System (SDCS) has been designed as a standalone system for screening, filing, and rapid retrieval of textual and non-textual data. In the standalone configuration the system includes a large content addressable disk file, the SCAT Associative/Parallel (A/P) Processor, a large screen graphics display terminal, a PDP-11/45 host, and associated peripherals. Alternately, the A/P Processor with disk file and/or graphics terminal can be supplied separately as peripherals to an existing non-dedicated host.

In either configuration the system can be programmed for the following capabilities:

- Real-time purge/update in non-indexed 300 Mbyte file expandable to 1.2G bytes. The system can handle data input rates up to 3000 char/sec. at 50% host CPU load.

- Screen input messages against many keyword analyst interest and/or priority profiles with real-time purge/update and/or dissemination. The system can screen messages at the 3000 char./sec. input rate against approximately 100,000 keywords.

- Compile search and retrieval programs for 1-32 keys/keywords. The system can handle up to one search request per second at 50% CPU load.

- Execute search programs using =,>,<, DONT CARE compare operators and their negatives and using AND, OR, EXOR, WITHIN, link operators and their negatives plus 7 levels of parenthesis. Average search speed is about 2.5 million characters/second.

- Retrieve and disseminate selected record attribute data on-the-fly for display in real time hit lists at analyst positions. The system can handle data retrieval rates of 300,000 char./sec. at 50% CPU load.

- Display hit lists or entire hit records or messages on analysts display terminal as requested. The system can handle three 4500 character dumb terminals or many 4500 character smart terminals at 50% CPU load.

The actual capabilities of the system in the standalone configuration at up to 100% CPU loading or at up to, say, 10% CPU loading of a non-dedicated host will be determined by input data rate, input data screening requirements, number of analysts

supported, search request rate per analyst, and the amount of data retrieved per search.

2.1.1 Standalone Configuration

In this configuration with the currently planned software, this system would handle a data base similar to the NMIC 5-day message file. The file would be loaded in the batch mode via RK-05 disk pack, paper tape reader, or terminal keyboard. The SA 500 Graphics Terminal would be used for the creation of file search and retrieval algorithms and for the display of retrieved messages or designated portions thereof. The system contains the following major components:

- Large Screen Graphics Display
- Content Addressable File
- Associative/Parallel Processor
- PDP-11/45 Processor and Associated Peripherals

Figure 2-1 shows the general organization of the system, and Figure 2-2 shows its mechanical configuration.

2.1.1.1 Large Screen Graphic Display

A Sanders SA 500 large screen (12" x 12" viewing area) graphic display provides the analyst with a method for the composition and editing of search and correlation algorithms as well as for the softcopy presentation of retrieved data. The graphic capability of the SA 500 allows for the potential display of search algorithm logical flow charts as well as for graphic (e.g., bargraph) presentation of selected data attributes. The display indicator with, alphanumeric/function keyboard and lightpen, is provided in a desk top unit measuring 21" high, 36" deep and 24" wide. The associated Display Generator Unit is housed in a 10½" high 19" rack mounted assembly.

The SA 500, as a general purpose caligraphic display, allows for extensive potential expansion of system alphanumeric and graphic presentations.

2.1.1.2 Associative Disk File (ADF)

The ADF provides for the storage of nearly 300 million bytes of data representing approximately 50 days' worth of formatted teletype messages. The ADF 4-track parallel READ/WRITE capability provides a high, continuous file readout rate of approximately 4 bytes/microsecond. Thus, an entire 300 MByte file can be read out (i.e., flushed) in approximately 75 seconds.

The disk unit utilized in the ADF is a Control Data Corporation 9790, housed in a 45" high x 45" deep x 22" wide cabinet. The disk control unit, designed by Sanders Associates, occupies three cards in the Associative Processor chassis.

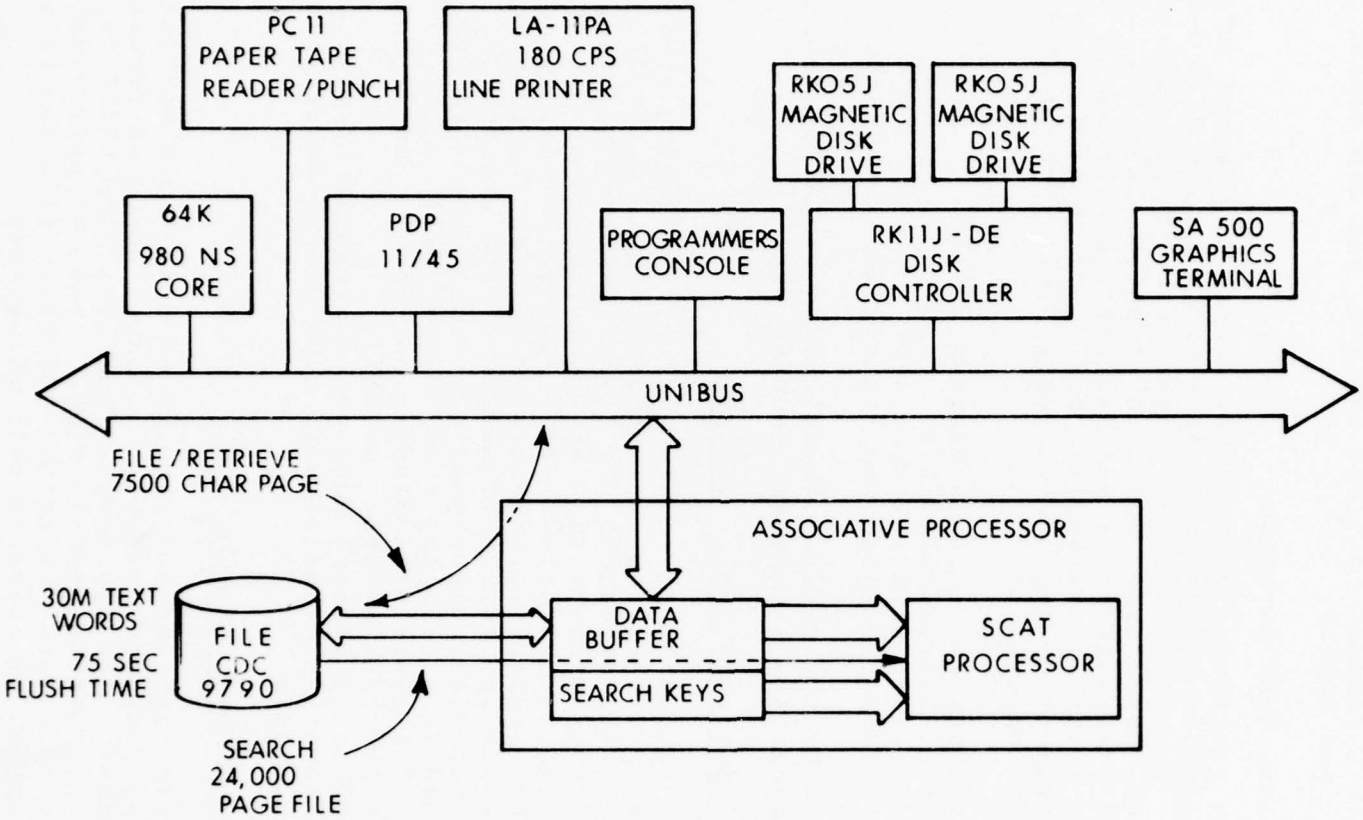


FIGURE 2-1
SYSTEM DETAILED BLOCK DIAGRAM

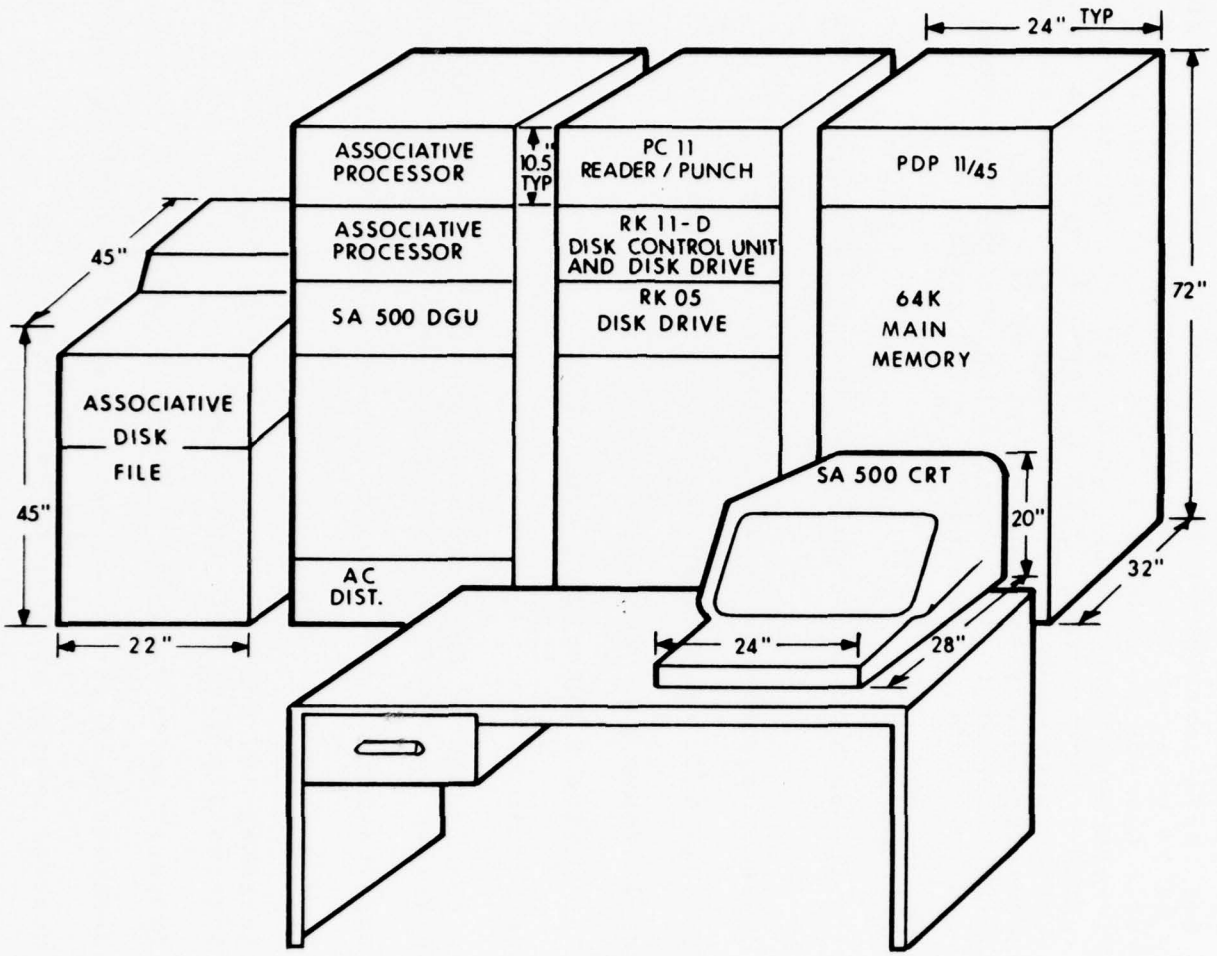


FIGURE 2-2
SCAT 16 SYSTEM CONFIGURATION

2.1.1.3 Associative/Parallel (A/P) Processor

The A/P Processor is a specially designed processor which provides for rapid correlations/searches to be performed on ADF data. Up to 32 bytes of key can be correlated with each byte of data while the ADF is read at its maximum continuous rate of 4 bytes/microsecond. For average text, with the processor by-passing unproductive records, up to 32 keywords used in a search can be compared with each textword of file data without slowing the 4 byte/microsecond data transfer rate of the ADF.

The A/P Processor is contained within one 19" rack-mount card cage, with a total of sixteen 7" x 10" cards.

2.1.1.4 PDP-11/45

The following hardware complement is associated with the PDP-11/45.

- System controller with 64K of 980 NS memory
- Two RK-05 2.4 MByte I/O disk with controller
- PC-11 Paper Tape Reader/Punch
- LA-11 Line Printer with Controller
- Decwriter

This complement of equipment, supported by the DEC RSX-11M operating system plus special SCAT system software, provides for:

- Application program creation, maintenance and storage
- Source data storage
- Encoding and formatting of source text inputs for Associative Disk File updating.
- Preparation of data for display on the SA 500
- Generation of search algorithms based on analyst inputs
- General system monitoring and control

2.1.1.5 System Software

Support Software

The RSX-11M operating system provided with the PDP-11/45 provides real time event driven multi-tasking support. System components include:

- Real time executive for interrupt handling, program fetch and dispatch, and I/O control.
- Full ANSI FORTRAN IV and Macro-11 languages for program development.
- File management system for storing and maintaining data, with access via symbolic identifiers.
- ODT (On-line Debugging Technique) which allows interactive execution of programs to locate faults.
- A text editor, EDIT-11, to assist in the creation and maintenance of program source files.
- A task builder program which collates relocatable object programs and prepares files suitable for execution.
- A number of general purpose utility programs such as the peripheral interchange program (PIP), file verification utility and a library maintenance program (LBR).

System Software

SCAT is provided with special software for operating the system in the standalone mode, with batch loading of fixed and free format data bases. Included are:

- Text formatter/deformatter including "tuckword" dictionary.
- Teletype header formatter/deformatter.
- Disk loader, including sector hard error dictionary for the disk file.
- Input displayer for composing and editing search algorithms on the CRT.
- SCAT Compiler

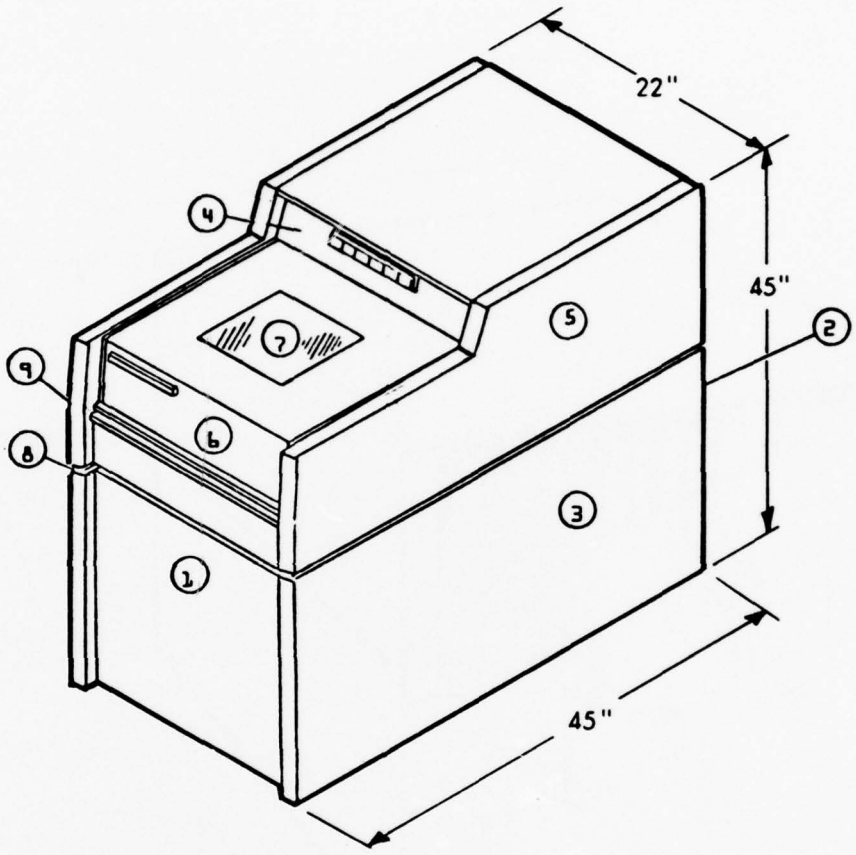
Terminal Support Software

The SA 500 is provided with the GSS-3 software support package which is incorporated into RSX-11M for display control. Functions included are: display control for text, vectors, points, & circles; input control from lightpen, trackball, & keyboard; scaling, clipping, and smoothing. GSS-4 provides the same set of services for the Graphic 7 most of which resides in terminal firmware. The rest resides in the host as FORTRAN callable subroutines.

2.1.2 Non-Dedicated Host

For operation with an existing or planned non-dedicated host computer; such as the PDP-11/45, PDP-11/70, or AN/GYQ-21(V); the ADF, A/P Processor, and graphics terminal could be provided separately in a Tempest qualifiable configuration. For this application the Sanders Graphic 7 Smart terminal would replace the SA 500 dumb terminal to minimize CPU loading of the host. Both terminals utilize the same Sanders model 530 CRT display and keyboard layout but the Graphic 7 DGU contains a microprocessor with 4K word ROM and 8K - 24K word RAM for display refresh memory and FORTRAN callable display control under standard GSSIV operating software and SCAT applications software.

Figures 2-3, 2-4, and 2-5 show the mechanical configurations of the DSU, A/P Processor, and Graphics Terminal respectively. Figure 2-6 shows how these elements would be integrated into a typical I&W system with the Message Support System hosting the A/P File and Processor with about 6000 SCAT instructions and the User Support System hosting the Terminal with a small number of SCAT instructions.



ASSEMBLY

1. FRONT DOOR
2. REAR COVER
3. SIDE PANEL
4. CONTROL PANEL
5. TOP COVER
6. PACK ACCESS
7. COVER GLASS
8. BELTLINE
9. TRIM STRIP

WEIGHT : 800 lbs
POWER : 208 VAC, 60 Hz
3.5 KW MAX.
10,000 BTU/HR. MAX

FIGURE 2-3

DISK STORAGE UNIT

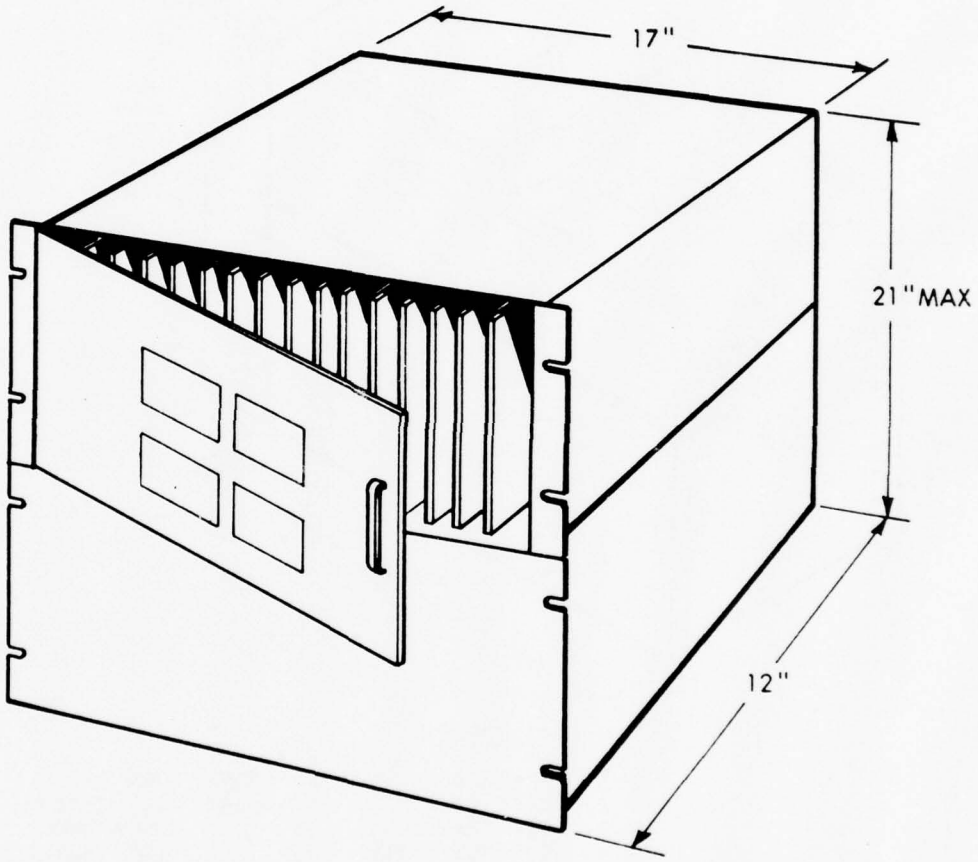
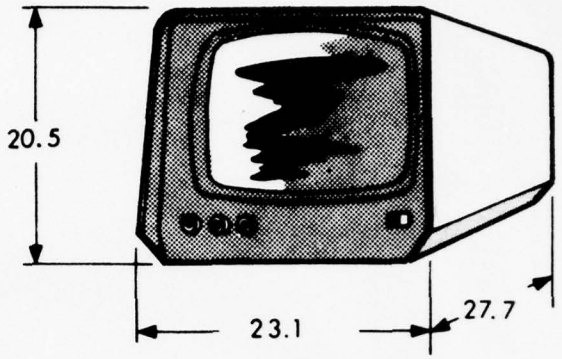


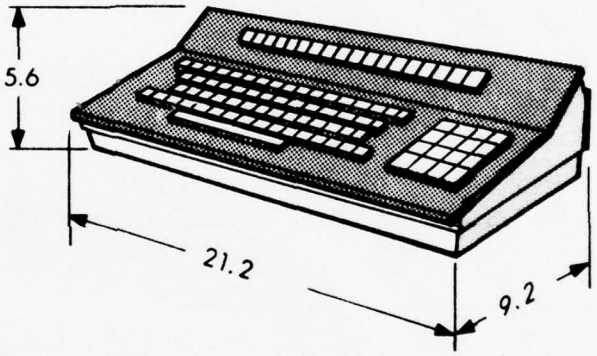
FIGURE 2-4

A/P PROCESSOR

MODEL
530
DISPLAY
INDICATOR



MODEL
2785
KEYBOARD



MODEL
5710
TERMINAL
CONTROLLER

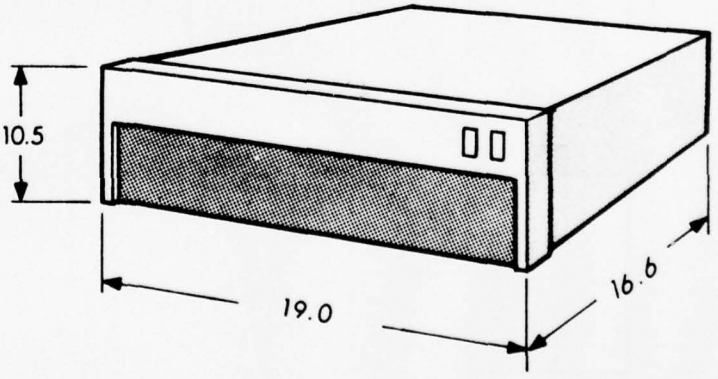


FIGURE 2-5

GRAPHIC 7 COMPUTER GRAPHICS DISPLAY SYSTEM

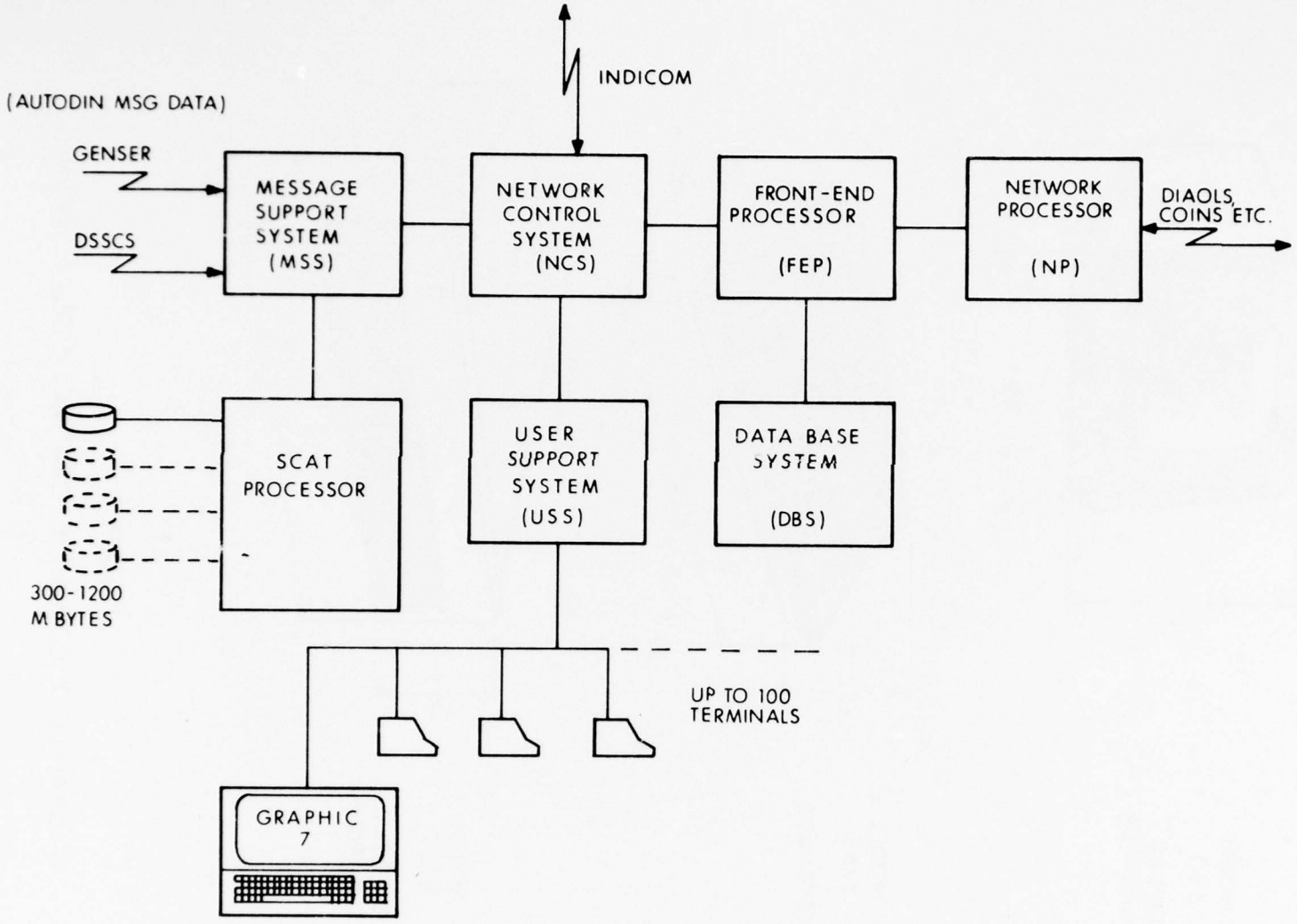


FIGURE 2-6 INTEGRATION INTO TYPICAL I&W CENTER

2.2 SYSTEM OVERVIEW

The SCAT A/P File and Processor is designed as a large intelligent mass memory peripheral to the PDP-11 family of minicomputers for the storage and fast, accurage retrieval of both textual and non-textual records. The file requires no directories or indexes because records are retrieved based on specific content and not their location in the file.

Because the file requires no directories, a large burden is removed from the host in purging and updating the file. In the SCAT system the file is partitioned into 24K pages (i.e., disk sectors) of 12K bytes each. A copy of the oldest page in the file is maintained at the host and is purged of all messages which are to be removed from the file. New messages are accumulated in this page until the page is full. It is then transfered to a 12K byte random access data buffer for the file and entered back into its former position.

To retrieve all messages relating to a given subject the analyst composes on his CRT a Boolean English search and retrieval algorithm containing all combinations of keywords which he believes will retrieve only messages of interest. The search algorithm is then compiled and transferred to a 4K byte random access program memory where it can be repeatedly transferred to the associative array. The disk then seeks the first sector where records of interest are stored and a continuous transfer of data from the disk to the associative array via the data buffer is made until the last sector containing records of interest is reached. Search & retrieval times are short because of the parallel architecture of the machine. During a search file data is continuously transferred from disk on four parallel tracks at a time at a combined average bit rate of 32 Mbps or 4 8-bit bytes per microsecond. The content of the file records is examined at the byte level in a rectangular associative array processor of 16 parallel data bytes by 8 parallel key bytes. To further speed the search process, the machine is designed to skip over unproductive records. The Associative Processor is fast enough so that search algorithms employing up to 32 search keys or keywords can be executed without interrupting the 4-byte/μs data flow from the disk.

The retrieval algorithm transfers requested data from hit records on-the-fly to the host computer or CRT terminal so that the retrieval process also does not interrupt the disk data flow. With a minimal amount of file organization to limit the portion of the disk searched, all data relevent to the search can be transferred to the host or terminal in a few seconds.

Figure 2-7 illustrates both the purge/update operation and a retrospective search. If the input message rate is 3000 175 word messages/day (about one every 30 seconds) it will require about 200 seconds to accumulate the 7500 characters which is the approximate net capacity of the 12K byte page. When the page has been filled it will then be filed on disk and, if all of the old

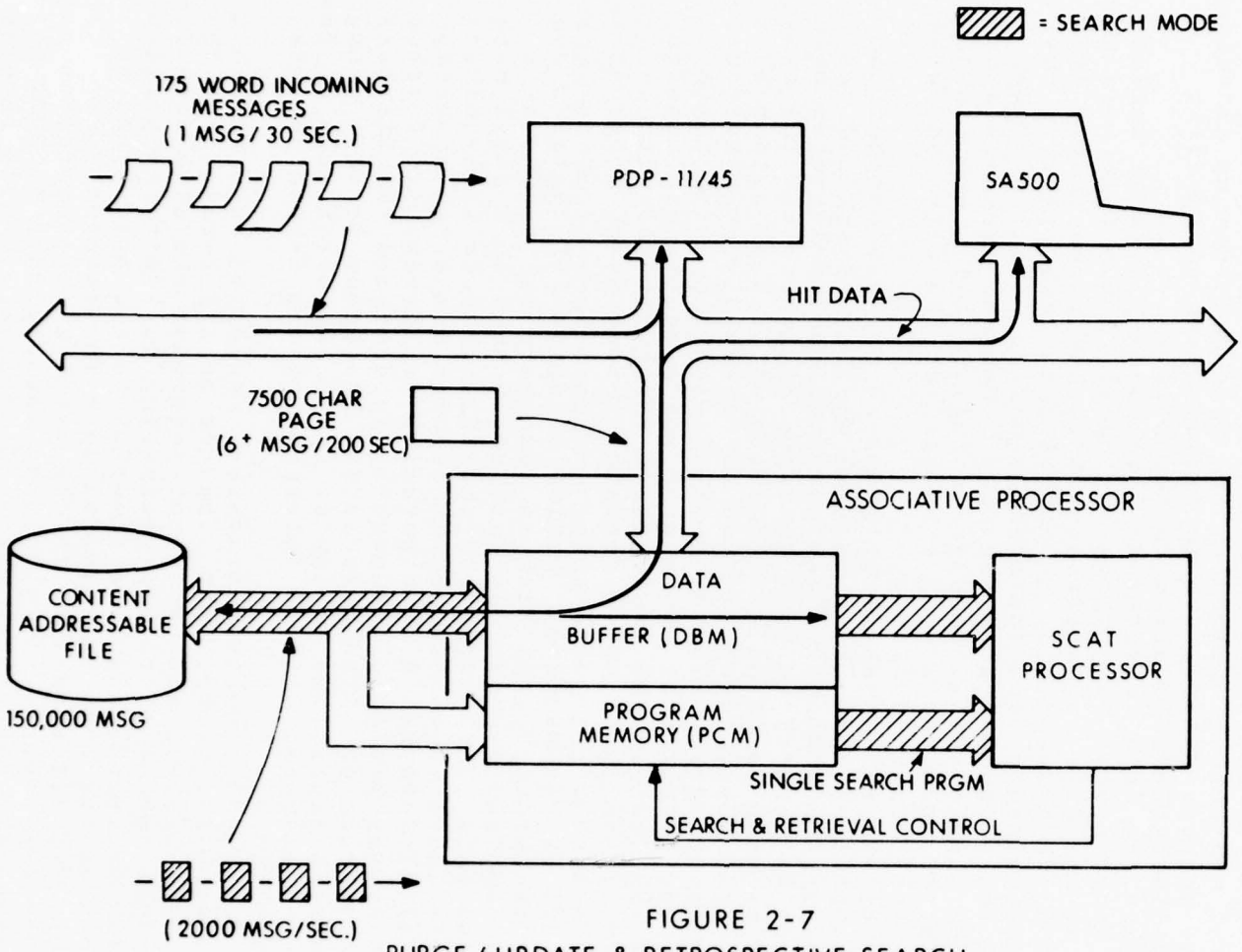


FIGURE 2-7
PURGE / UPDATE & RETROSPECTIVE SEARCH

messages are not to be purged, this update will occur more often. In order to be able to retrieve a message immediately after receipt, it is temporarily stored in a buffer sector until the next update operation occurs.

The SCAT system is designed for easy entry of search and retrieval algorithms by the analyst at the CRT terminal. Thirty-two special function keys are provided for analyst command of the system and for entering the Boolean compare and link functions required for the search algorithm. Algorithms may range from simple lists of keywords to sophisticated structures involving header data, word phrases, words which must not appear, word stems, and alternate combinations of keywords which will satisfy the intent of the search. The utility of the system and the accuracy of retrieval is adaptive to the analyst's mastery of the technique of conducting searches by specific content.

Retrieval algorithms determine what data is to be retrieved from records which meet the requirements of the search. For teletype messages this may range from a simple listing of the date and originator of the hit messages, a listing of keywords which caused the hit, to sequential presentation of the entire hit messages. In a file of tactical sensor target reports selected data (such as latitude and longitude of the target, time of the report, and sensor type) can be extracted on-the-fly on the basis of area of interest, target type, target emissions, etc. This data could be presented on a map underlay for rapid, operator assisted correlation of target/sensor data. This operation is illustrated in Figure 2-8.

Search and retrieval algorithms which are to be repeatedly used can be stored on the disk for later retrieval and execution. In fact, since the disk can feed either the program memory or the data buffer memory, the roles of the two memories can be swapped so that a block of 12K bytes of data in the data buffer can be continuously compared to search keys/keywords previously stored on disk and continously transferred to program memory. Thus, analyst keyword profiles by subject interest and subject propriety profiles of any length can be stored on disk and used to screen each incoming message as it is input. Messages which meet any of the profile criteria can be selectively filed and/or disseminated as shown in Figure 2-9.

Detailed specifications for the Disk Storage Unit, the Associative Processor, and the Graphic 7 Display Terminal are presented in Tables 2-1, 2-2, and 2-3 respectively.

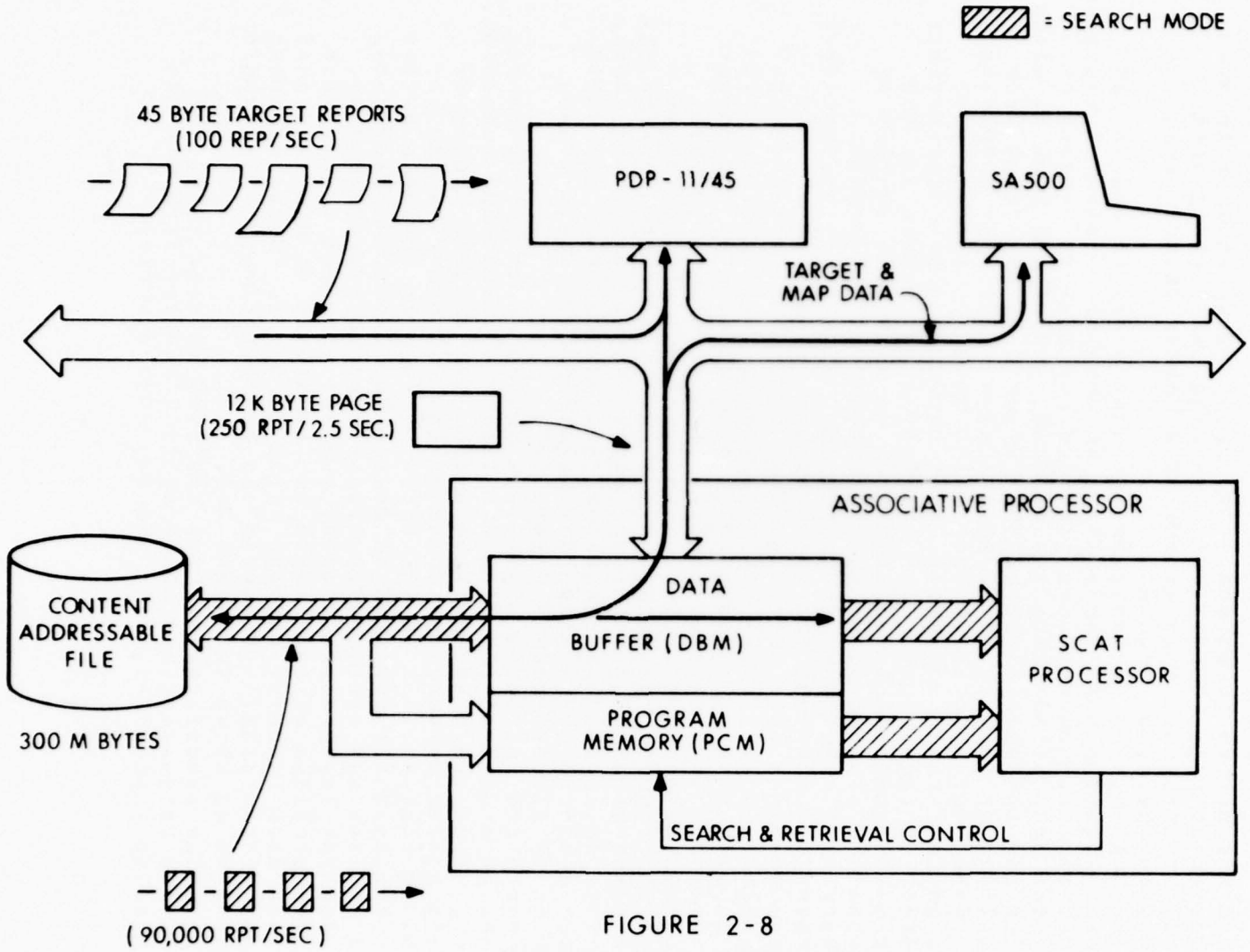


FIGURE 2-8
SENSOR DATA CORRELATION

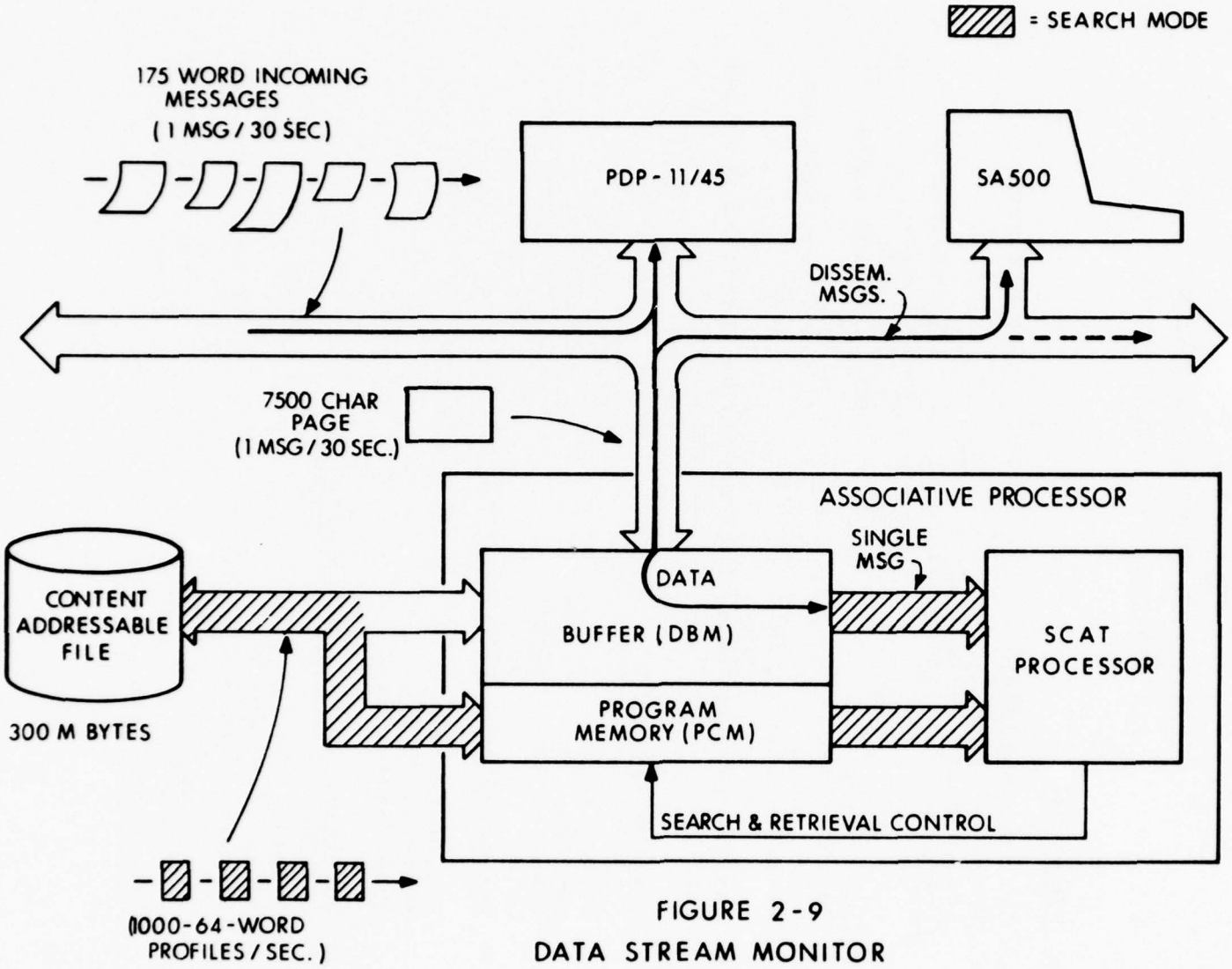


FIGURE 2-9
DATA STREAM MONITOR

TABLE 2-1

SENSOR DATA CORRELATION SYSTEM

DISK STORAGE UNIT SPECIFICATION

- General

Cylinder/Spindle:	404 + 7 spare
Tracks/Cylinder:	40
Active Heads/Cylinder:	4
Cylinder Seek Time (ms):	15, TRK-TO-TRK*
	50, AVER.
	80, MAX.
Size (in):	45H X 45K X 22W
Weight (lb):	800
Power (kw):	.750 nom, 3.50 max.
Rotation Period (ms):	16.67

* TRK-TO-TRK Seek Time shall always be less than rotation period.

- Unformatted Data

Bytes/Track:	20,160
Bytes/Spindle (411 cyl.):	331,430K
Transfer Rate/Track:	1.209M Bytes/Sec.

- Formatted Data (Single Track)

Sectors/Track:	6
Bytes/Sector:	3072
Bytes/Sector Gap:	288

- Formatted Data (4 Track Parallel)

Bytes/Sector:	12,288
Sectors/Cylinder:	60
Transfer Rate/4 Tracks:	4.0M Bytes/Sec Cont.

- Static Skew: 1 µs max. (10 bits)

  Skew after head change: 5 µs max. (50 bits)

TABLE 2-2

SENSOR DATA CORRELATION SYSTEM

ASSOCIATIVE PROCESSOR SPECIFICATION

1. Principal Functions

1.1 Store digitally coded textual or fixed format messages on the basis of time of arrival.

1.2 Retrieve all or selected parts of these messages on the basis of fixed format attribute values and/or textual content.

2. Basic Description

The Associative Processor (A/P) is an intelligent two-port controller. The computer port adapts the A/P to a host mainframe, where it accepts information for storage and receives search queries. The data base port interfaces to a mass storage device. The prototype A/P is designed for use with Digital Equipment PDP-11-X host and a Control Data CDC 9790 disk storage unit, but with the replacement of the adapter modules may be used with other mainframes and storage units.

3. Computer Port Specification

3.1 Data	
3.1.1 Structure	16 bit Parallel Word
3.1.2 Protocol	Asynchronous Selection/Acknowledge
3.1.3 Transfer Rate	$0\text{-}10^6$ words/second bidirectional
3.2 Address	
3.2.1 Structure	20 bit Parallel, Bidirectional
3.2.2 Protocol	Asynchronous Selection/Acknowledge
3.3 Control	
3.3.1 Interrupts	Processor Interrupt-Programmed Input/Output
	Non Processor Interrupts Direct Memory Access (DMA)
3.3.2 Polled Operation	Sixteen bit readable Status Register

TABLE 2-2 CONT.

4.	Data Base Port Specification	
	4.1 Data	
	4.1.1 Structure	4 serial channels
	4.1.2 Protocol	Synchronous
	4.1.3 Transfer Rate	9.7MHz each channel Bidirectional
	4.2 Address	24,240 directly addressable sectors 12,288 bytes/sector
5.	Data Buffer	
	Capacity	12,288 bytes
	Organization	768 x 128 bits
	Transfer Rate (peak)	6.6 bytes/us bidirectional
6.	Program Buffer	
	Capacity	4,096 bytes
	Organization	256 x 128 bits
	Transfer Rate (peak)	6.6 bytes/us bidirectional
7.	Search Control	
	7.1 Hit Response Options	Stop on hit Increment hit counter Fetch Message Location Fetch Message Header Fetch Message Fetch Key Strike Register
	7.2 Byte Level Operators	Data byte = Key Byte Data byte ≠ Key Byte Data byte < Key Byte Data byte > Key Byte Data byte ≤ Key Byte Data byte ≥ Key Byte Continued True Unconditional False
	7.3 Key words per search	1 - 32
	7.4 Bytes/Keyword	1 - 32
	7.5 Keyword Links	AND, OR, EXOR, NOT, NAND, NOR, EXNOR, PARENTHESIS (7 LEVEL)

TABLE 2-2 CONT.

7.6	Proximity of Non Tuckwords (QUOTE)	A field of within 2 to 8 non tuckwords.
7.7	QUOTE Groups	4- Two keywords at a time 2- 4 keywords at a time 1- 5-8 keywords at a time
7.8	Search Rate (no skip)	1-24 keys 4 bytes/us 25-32 keys 3 bytes/us
7.9	Search Rate (50% skip)	1-24 keys 7 bytes/us 25-32 keys 5.25 bytes/us

TABLE 2-3

SENSOR DATA CORRELATION SYSTEM

GRAPHICS DISPLAY TERMINAL SPECIFICATION

- TERMINAL CONTROLLER

  General

Power Source:	115± 10 Vac, 47-63 Hz
Power:	300W
Temperature:	Storage: 0 to 50°C Operating: 15 to 40°C
Relative Humidity:	10 to 90%
Dimensions:	10.5 in. H, 19.0 in. W, 16.0 in. D
Weight:	55 lbs

- DISPLAY PROCESSOR

  General Purpose Microprocessor

Word Length:	16 bits
Byte Mode:	8 bits
Instructions:	400+
Registers:	8

  Automatic Priority Interrupt

  Memory

ROM:	4K words
RAM:	8K to 24K words

- HOST INTERFACE

Parallel:	16 bits, 500K words/sec. (TTL standard)
Serial:	RS 232C, 9600 baud standard (up to 50K baud optional)

- GRAPHIC CONTROLLER

Parallel Microprocessor:	16 bits
Display Instructions:	40

  Synchronized Linkage to Display Processor

TABLE 2-3 CONT.

Subroutine Stack	
Display Registers:	13
GP Registers:	4
Refresh Rates:	60, 40 or 30 Hz; or free running

- VECTOR/POSITION GENERATOR

Addressable Locations:	2048 by 2048
Viewing Locations:	1024 x 1024
Line Type:	4
Programmable Speeds:	2
Adaptive Timing	

- CHARACTER GENERATOR

Type:	Cursive Stroke
Character Set:	96 Standard, 96 Optional
Aspect Ratio:	3:2 (normal)
Rotation:	90° counterclockwise
Sizes:	4
High Speed:	2.4 usec (typical) 3.6 usec (with tab)
Programmable Speeds:	2
Character Write Time:	150 nsec/stroke Adaptive Timing

- OUTPUT CHANNEL

Total Displays:	4
X, Y Channels:	$\pm$ 5V
Z Volts:	0 to 1.5V
Termination:	75 Ohms
Brightness Levels:	8
Blinking (adjustable)	0.5 to 5.0 Hz
PHOTOPEN Intensifier	

TABLE 2-3 CONT.

- DISPLAY INDICATOR (MODEL 530)

Viewing Area: (max.)	12 x 16 inches
CRT:	21 in. diagonal
Positioning Time:	25 μsec
Position Accuracy (% of full scale)	± 1%
Position Repeatability: (% of full scale)	± 0.1%
Contrast Ratio:	4:1
Line Width, Spot Size:	0.02 in.
Power:	275W
Approximate Size:	24 x 24 x 24 in.
Weight:	98 lbs
Phosphor:	P31 (Green); others available
Recommended Refresh Rate:	60 frames/second; line locked
Ambient Lighting:	40 foot candles on horizontal work surface
Deflection:	Electromagnetic, using Sanders patented write-through-yoke techniques.
Focus:	Low voltage electrostatic
Controls:	Brightness, contrast, focus, power ON/OFF
Cabling:	50 ft. coaxial supplied for X, Y and Z from terminal controller

2.3 System Functions

2.3.1. General Capabilities

The Sensor Data Correlation System (SDCS) is designed to allow an analyst to compose search algorithms and execute them to find each message from the input or permanent data base which matches the criteria of the algorithm. The analyst may edit messages from the data base and refile the edited message in the active input area or in a permanent storage area.

The input data base for the system will be created from messages which have been stored on a removable disk pack by another PDP-11 system. In the future, the system could be modified to accept input from a direct UNIBUS* interface or a modem communications interface. For test purposes, messages may also be entered from the display keyboard by editing a null message.

The analyst may enter a search algorithm and a file to be searched and then initiate a search to find and display a list of the accession numbers of all messages within the file or files which match the search algorithm. Selected data from the message header and/or the hit mask may be displayed with the list.

2.3.2 Search Algorithm Entry and Edit

A search algorithm is a group of header attribute values and text keywords joined by link operators. It specifies the content of the group of messages that the analyst desires to examine.

The analyst enters search algorithms via the display keyboard. The display will show the portions of the algorithm which have been entered and also assist in positioning and choosing the next entry. The algorithm consists of one format term and at least one attribute or text term. Typically there will be several attribute and text terms. Each term is joined to the previous term by a link operator. Parentheses may be used to group the terms.

Format Term

The first term of each search algorithm will be a format term. The term consists of only the format name on a line by itself. A search algorithm can search only messages of one format so each algorithm has one format term as the first term.

Initially the system will have only one format defined, others may be added.

Attribute Terms

An attribute is one of the fields of the message header which may have only predefined values. The values are either numeric, such as date, time, message number; or named such as source, addressee, category code.

An attribute term allows the system to search for a value of one specific attribute. It may be a single value, up to eight unique values, or if the attribute is numeric, a range of values. The attribute terms, if any, must follow the format term and preceed any text term.

An attribute term generally consists of a single line containing: a link operator, an attribute name, an attribute operator, and a value or values.

- Attribute Name

  The attribute name is a name of one of the message header fields. In the format definition table, each attribute will be defined as named or numeric and as single or multi-valued. A multi-valued attribute may have up to 8 values.

- Attribute Operator

  The attribute operator is one of the following operators which is permitted for the given attribute name. Optionally, "NOT" may be used to prefix any of the operators.

OPERATOR	PERMITTED VALUE(S)
1. equal to	1 to 8, named or numeric.
2. greater than	one numeric only.
3. less than	one numeric only.
4. between	two numeric only.

- Attribute Values

  The operator specified will determine how many values will be accepted. The attribute name will determine if numeric or named values will be accepted and if the attribute is single or multi-valued. In the list above, the permitted values are indicated.

"Equal to" permits one to eight values which may be either named or numeric. Values are separated by commas if any value will satisfy the search. For multi-valued attributes, ampersand (&) may join values where all values must be present to satisfy the search.

"Greater than" or "less than" permits only a single numeric value.

"Between" permits only two numeric values. The end points of the specified interval will be included.

Text Terms

A text term consists of a list of one or more words or phrases, called elements, separated by commas and terminated by a period. The list of elements may occupy more than one line. A phrase is two to eight words separed by spaces. The elements separated by commas are linked by the inclusive OR operator. A text term is satisfied (matched) if any element is found in the messages being searched. A phrase must be matched by the same words in the same order with no intervening words or punctuation.

- Characters and Punctuation

  The letters A thru Z and the numbers 0 thru 9 will always be considered characters. Some punctuation such as & % $ # @ will also be treated as characters, that is "32%" or "#99" will be treated as three character words.

  Others will be determined by context. For example, period, comma, slash, and... followed by space will be punctuation but if preceeded and followed by numeric characters, they will be treated as characters, thus "34,749,423", and "0.003" will be words.

  Exclamation mark, question mark, parentheses, brackets, braces, double quote, colon, semi-colon, asterisk will always be punctuation.

- Wildcard Characters

  A word is a string of adjacent characters terminated by a space or punctuation character.

If the word to be searched for may have several endings or possible spelling variations, "don't care" or wildcard characters may be used to construct the key word for the search.

The question mark (?) is used to represent exactly one single don't care character. The crosshatch (#) is used to represent either zero or one character. The asterisk (*) is used to represent any number (zero, one, or many) of don't care characters at the end of a word only.

For example:

Keyword:	Will Match:
LAUNCH*	LAUNCH, LAUNCHED, LAUNCHING, LAUNCHES, LAUNCH-PAD, ...
?OSMOS	KOSMOS, COSMOS, ...
REACT??	REACTOR, REACTED, ... but not: react, reacting, reaction, ...
REACT##	REACT, REACTS, REACTED, REACTOR, ... but not: reaction, reacting.
MAN*	MAN, MAN'S MANNED, MANNING, MANUFACTURE, MANIPULATE, ...

Link Operators

The link operator specifies the Boolean operation by which two terms or groups of terms are joined. Terms are grouped by means of parentheses which may be nested up to five levels. "NOT" may preceed and term or group of terms. The link operators are:

AND	
AND WITHIN --	(must join text terms)
OR	(must be in parentheses)
XOR	(must be in parentheses)

(The "AND WITHIN --" operator will allow a number of from 2 to 7 words to be specified. The count will include both matching words and any non-tuckwords between them).

- Algorithm Edit

  When an algorithm is displayed, whether during entry or later, the analyst may insert or delete a term or any part of a term or its link. This is done by positioning a cursor to the part to be changed and using function keys to enter, modify, or delete the item.

2.3.3 Storage and Retrieval of Search Algorithms

The system as delivered will be able to store search algorithms or partial search algorithms. These algorithms may be recalled by the analyst and displayed for edit or execution. The analyst can name algorithms as they are stored and recall them by name or display the list of those stored. Optionally if the algorithms are stored on the Associative Disk File (ADF), keyword searches may be done to find algorithms.

2.3.4 Search Algorithm Compilation

After an algorithm has been entered, and edited if desired, it must be compiled before it can be executed. The compilation process will indicate any errors or warnings to the analyst by blinking or otherwise identifying the name, word, or operator which caused the error.

The compiler will accept the search algorithm input by the analyst and translate it into an associative processor search program consisting of header attribute value blocks and text keyword blocks, link operators, quote field qualifiers, and the header attribute location data.

The compiler will sort and modify the input and display the modified algorithm. It will also produce a program to define the search to the associative processor.

Value and Keyword Validation

As the first step, the compiler will look up each named item (format, attribute, value) and verify that the name is valid. The program codes for each name will also be obtained. Each text element (word or phrase) will be compared to the tuckword dictionary entries. Tuckwords which follow non-tuckwords in phrases will be encoded. Note that tuckwords may neither begin a phrase nor be a single word element.

Keyword Sort

The compiler will sort the text keywords and the attribute values into the proper order for the search program. This sort will insure that all attribute values occur before any text keywords and that any keywords which appear in quote fields are within the first eight text keywords. This may require inserting additional parentheses and duplicating certain keywords within the groups formed by the parentheses and/or modifying the link operators in order to preserve the logical relationships of the original algorithm.

- Errors detected during this phase will include:

  Attribute terms cannot be grouped and linked to text terms.

  Text search cannot be divided into blocks of less than 8 keywords.

Syntax and Key Limit Analysis

The keywords, attribute values, parentheses, and link operators in the sorted search algorithm will be examined to determine if they can be blocked into a search program. This will require blocking the search algorithm so that the following limits are not exceeded:

- There may be no more than four program blocks. A block may contain eight text keywords or eight attribute values, values and keywords may not be mixed within a block.

- Each block must have its elements combined into a signel logical group.

- The first text block must contain all keywords which appear in quote field specifications.

Quote Field Pattern Synthesis

The keywords within quote fields will be examined to see which combinations of words can be permitted in the text to match the search algorithm specification. The result of this will be the quote field bit mask for the search program.

Header Attribute Location

Location data will be retrieved from the format

definition table for each attribute. This data is also inserted into the search program.

2.3.5 Search Execution Order

The search execution order contains two items: 1) Where to look; and 2) what to do when a match is found. What to search for is described by the currently displayed compiled algorithm.

File Area Specification

Where to look is indicated by one or more file area names in the search execution order. If no name is specified, the search will cover all the messages stored.

Hit List Options

The minimum hit list will always contain the accession number of each hit and its location on the ADF. The location data will not be displayed but will be used if the operator requests a display of the full message.

Optionally the operator may specify additional information to be put into the hit list. The items which may be included are:

- full header
  - date
  - time
  - message ID
  - source
  - category codes
- full text
- file name in which hit was found
- hit mask showing which keywords were contained in each hit.

Note that if several items or the full text is requested, the list may be filled by the first few hits and no data pertaining to later hits will be available. In any case even with the minimum hit list, a count of the total number of hits will be included and an indication if there were more hits than would fit in the list area.

2.3.6 Message Storage Areas

The Associative Disk File (ADF) has a capacity of

300 megabytes in 24,240 sectors of 12,288 bytes each. File areas are assigned a name and a fixed physical location. The system as delivered will have only the active file area defined but others can easily be added. A named area can either be a single file area for search or entry, or it may be a group of adjacent file areas for searching only.

Active File Area

This area will be large enough to accommodate at least six days input messages under most circumstances. If message traffic is higher than expected, or if longer retention times are desired, the area assigned to this file can be increased. Messages will be deleted from this area only as new input is received which requires the space. If input is slow, messages may remain on the active file more than five days. Optionally a routine may be added later to delete messages exactly five days after their entry into the system.

The active file will have its cylinder allocations updated automatically as messages are added. This is the only file area which will have this feature. The active file area will have several names associated with it. One will be for the entire active area and the others will be for each of the most current five days. The oldest messages will be overwritten as new data is added. Messages which are to be retained longer should be copied to a permanent file.

Permanent Storage Areas

The remainder of the ADF not occupied by the active file may be used for permanent files. It may be divided into file areas for messages and commentary which the analysts desire to retain. The file areas will be assigned names and allocated a certain area of the ADF. Messages of interest which are found in the active file may be edited by the analysts and filed in one or more of the permanent areas. These files may be reserved for geographic areas, individual analysts, subject codes, or any other criteria desired by the analysts. Messages in the permanent file areas will not be deleted except by specific analyst action. Optionally a routine could be added later to periodically purge messages of more than a certain age, such as 90, 180, or 360 days.

2.3.7 Message Input

Input messages for the five day file are accepted without any requirement for action by the analyst. There will be a log of input execution reports which will call out input messages which did not correspond to the prescribed message format or had invalid entries in the header fields. The file area directory for each days input will be automatically updated. As the area allocated to the active file is filled, new input will write over the oldest messages still in the file. When a days messages have been written over, that day will be removed from the directory.

In the initial system, input will be read from files which have been placed on the RK-05 disk pack by another system. Optionally the system could be adapted to accept on-line input.

2.3.8 Message Editing and Refiling

The analyst may display and examine any message found either by search or by direct access if the message number is known. If desired, he may edit the message by modifying or deleting portions of the text and/or header. He may also add comments to the message. After editing, the message may be refiled in the active file or in one of the permanent storage areas by specifying a file area name in a file command. The file area specified must be a single file.

After each message is filed, the space remaining in the area will be reported to the analyst. He may delete one or more messages and/or request that the data be compressed so that space may be made available for new data. The space allocated to that file area may be increased in the file name directory if the operator observes that the space remaining is insufficient for future needs. Note that file directory changes can be made only when the terminal is inactive.

2.3.9 Name Directories

There will be several directories or lists of names which can be modified to change the actions of the system. Since access to data stored on the ADF can be affected by these changes, changes will not be permitted while the system is operating. It will be a simple task for User personnel acquainted with the PDP-11 to modify directories.

Tuck Words

The tuck word list will contain up to 160 punctuation symbols (. , " / ( ) -) and short words (such as "a", "the", "and", "is".) which are frequently used and not likely to be the subject of a search. These words should not be changed unless all messages stored on the disk are edited to reflect the new list. If all the codes have not been used, new codes can be added but this may cause messages which were entered before the addition not to match on a phrase search element. The added tuck word will not be permitted as a single word text search element.

Format Related Names

Initially the system will allow only one message format. Others can be added by inserting the appropriate format definition information, including:

1. The format name
2. The name, type, and location of each attribute in the header.
3. The allowable attribute values, either a numeric range, or a list of value names.

The format definition will also include data which are used by the computer to form the Associative Processor search program.

File Area Names

The allocation of storage in the ADF will be defined by the file area name directory which will contain the name of each file area and the tracks or cylinders allocated to it. The names and allocations of the active file will be updated automatically, but the User may specify the area allocated to all active files and the names and allocations of permanent files.

Search Algorithm Names

When each search algorithm is filed by the analyst, the name will be added to the list of algorithms on file. These algorithms will be stored on the RK-05 disk. This is the only directory which can be updated on line.

2.4 SYSTEM DATA FLOW

2.4.1 Data Types

There are four types of data associated with the SDCS. They are messages, search algorithms, message numbers and system files. Sources and destinations for these data types are the system disk (RK-05), the system terminal (Decwriter), Associative Disk File (ADF), Line Printer (LA-11), and the Graphics Display terminal (SA500).

2.4.2 Messages

Messages are stored in either teletype or associative processor format depending upon where they are residing. In general, messages stored on the ADF are blocked into associative processor format and messages on the system disk or the graphics display are in teletype format. ACP 127 (E), JANAP 128 (F), and other applicable standards will be used for formatting AUTODIN.

Messages are assumed to be input in teletype format complete with carriage returns and line feeds. Other inputs messages are assumed to be in standard ASCII Representation. The exact structure of these messages and the peculiarities of different installations can only be settled by direct interaction between Sanders programmers and user site representatives.

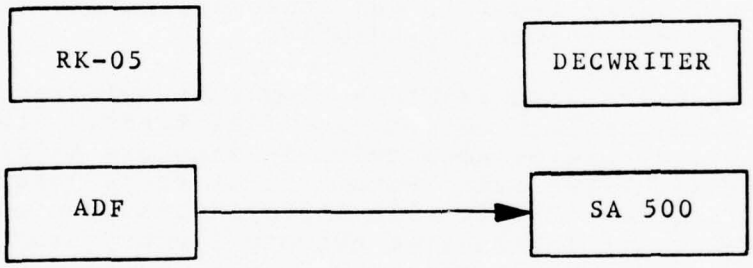
Input Message Flow

Initially the input device will be the RK-05 Disk. Input messages meeting the criterion set out in paragraph 2.1.3.2 are stored as logical records in an RK-05 Disk File. To input messages, the appropriate disk cartridge is loaded. The analyst specifies the UIC and filename of the file containing the messages. The new messages are blocked into associative processor format and stored onto the ADF.

Optionally, software may be written to support either the paper tape unit or a communications interface such as a modem as a message input device. This will be necessary for future real time applications. The input message flow is as follows:

Display Message Flow

To display a message stored on the ADF, the user specifies the message number and the message is retrieved from the ADF, unblocked, and displayed on the graphics terminal:

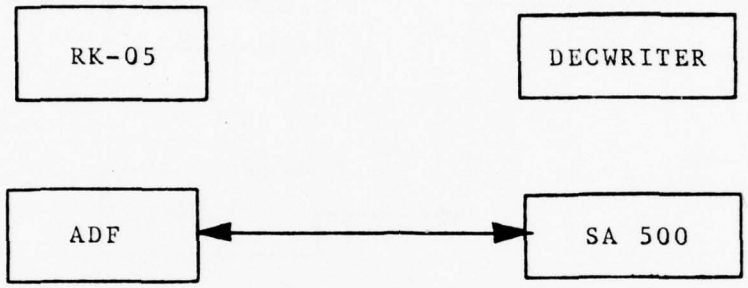


Update Message Flow

After editing a displayed message, the updated version is written back to the ADF. If the new version is longer than the old, the old message is deleted and the new one is written to a buffer area on the ADF. Else the new version is written over the old message:

Composite Message Data Flow

Messages originate on the RK-05 Disk. They are blocked and stored on the ADF during input. Then they can be unblocked and displayed on the Graphics Terminal, edited, reblocked and stored back onto the ADF.

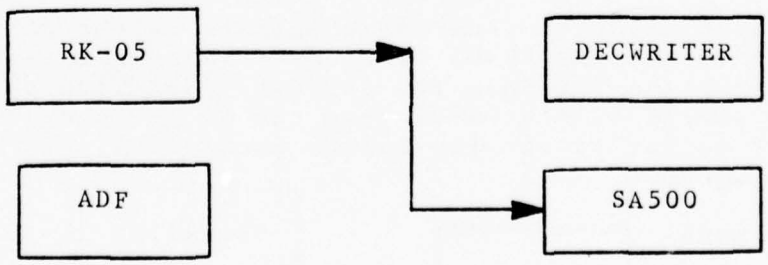


2.4.3 Search Algorithm

Both the sources and the compiled object of search algorithms may be stored on the system disk. Further, the source may be retrieved, edited, compiled and the updated version of the source and object stored back on the RK-05. The object files are transferred from the RK-05 disk to the buffer of the ADF to initialize the search.

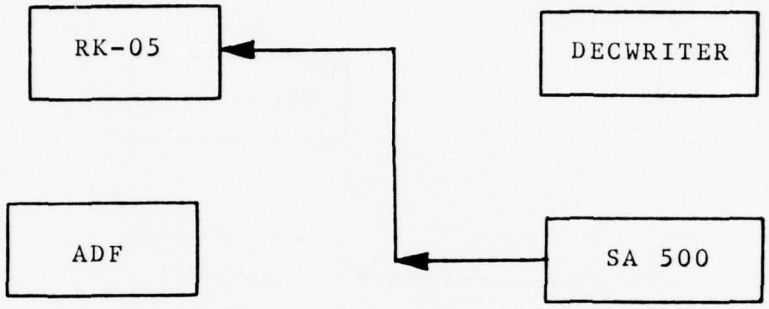
Retrieving Search Algorithms

To update a search algorithm previously stored, the source of that algorithm is retrieved from the system disk and displayed on the graphics terminal:



Storing Search Algorithms

After editing a search algorithm source and compiling the corresponding object code, both data files are stored on the RK-05 disk:

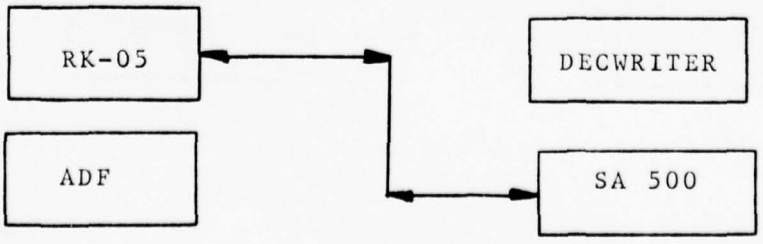


Exectuing Search Algorithms

To execute a search algorithm, the appropriate object module is transferred from the RK-05 disk to the program block area of the ADF buffer:

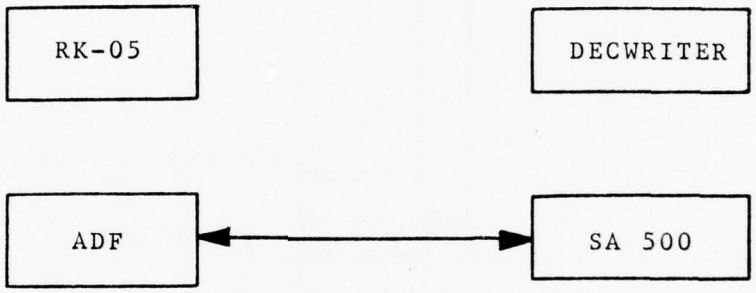
Composite Search Algorithm Data Flow

Search algorithm sources originate on the SA 500. are stored onto the RK-05 disk, and may be retrieved back to the graphics terminal for re-edit. Compiled object code is stored on the RK-05 from the SA 500 and is loaded into ADF buffer to specify search parameters.



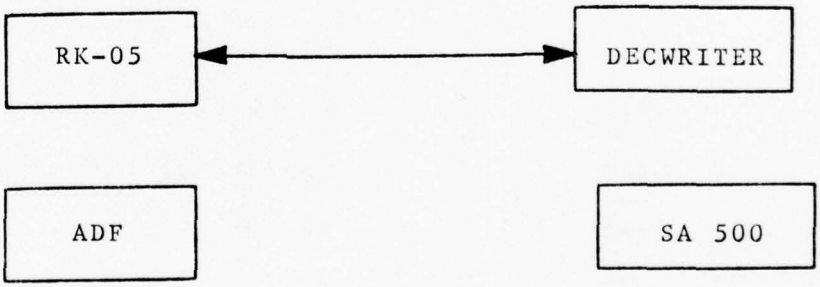
2.4.4 Hit List

The result of a search is a list of hits. The list contains message number and other identifying information. This list is produced during a search as hit data is passed from the ADF to the graphics terminal. Message numbers are also used in the display and update message functions to specify the appropriate message.



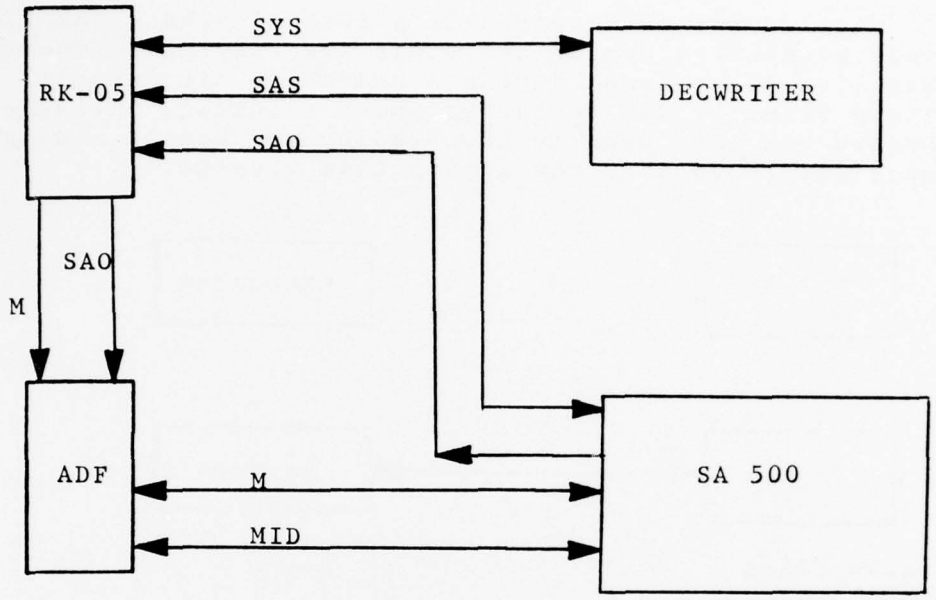
2.4.5 System Files

System files, primarily programs and indexes, are stored on the system disk and maintained from the system terminal under the RSX-11M operating system:



2.4.6 Composite Data Flow

Messages originate on the system disk, are stored on the ADF, displayed on the graphics terminal and restored on the ADF. Search algorithms are created on the SA 500, stored in User directories of the RK-05 disk and can be recalled to the ADF for further editing. Search algorithm objects are compiled from sources on the SA 500 and stored on the RK-05. From there they are loaded into the ADF to execute a search. System files flow between the system disk and the system terminal:



M	- Messages
MID	- Messages ID's
SAO	- Search Algorithm Objects
SAS	- Search Algorithm Sources
SYS	- System Files

2.5 Associative File and Processor Architecture

Functionally, the associative file and processor is a peripheral on the PDP-11 bus. Search algorithms and related search parameters are passed to the Associative/Parallel (A/P) processor, the search performed by the A/P processor, and search results passed to the PDP-11. The search process itself is an "off-bus" operation performed entirely within the associative processor unit.

The major components of the associative processor are the Content Addressable File and the A/P Processor with its associated disk buffer, bus interface, program memory and processing logic.

Figure 2-10 is a block diagram of the associative processor showing the relationship of its major components.

The SDCS disk file with input, output, and search logic resides in a collection of logic boards, cables and disk(s) known as the Associative Processor. This Assembly can be made to perform as a large (300 megabyte to 1.2 Gigabyte) random access mass storage medium or as a large data base, whose contents may be interrogated without the restrictions commonly associated with indexed data retrieval systems.

Physically, the Associative Processor is a 16-card 19" rack mountable logic card file. The Control Panel at the front of the card file is provided for entering diagnostic instructions and monitoring associative processor status. The card file with the associated Control Panel mounts onto one of the three PDP-11 equipment cabinets. A ribbon cable connects the Associative Processor (A/P) card file to the PDP-11 UNIBUS providing the A/P with the primary command and data link to the PDP-11 host. Another cable, the disk control cable, links the Associative Processor to a 300 megabyte Disk Storage Unit. More spindles at 300 megabytes/spindle may be added as customer requirements demand. The Disk Storage Unit is a semi-fixed medium, forty surface single spindle device. Disk transfers to and from the four heads take place over four 9.7 MHz serial data transfer lines within the disk control cable. Although the prototype system is based around a PDP-11/45, the Associative Processor is not restricted to this particular host. As a general computer peripheral, the Associative Processor, with suitable interfacing, can be adapted to other computing devices.

The sixteen logic cards of the Associative Processor can be classed into three distinct functional groups.

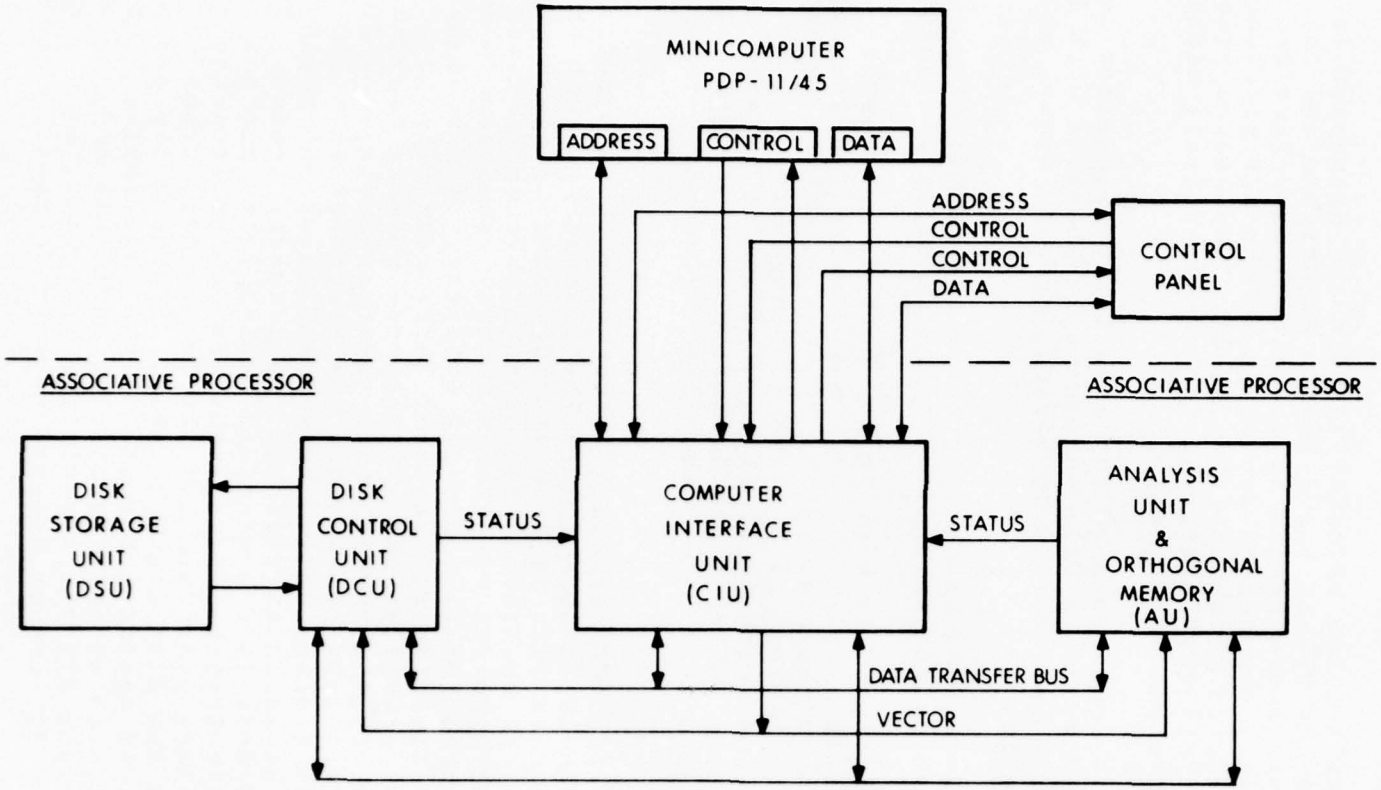


FIGURE 2-10
ASSOCIATIVE PROCESSOR BLOCK DIAGRAM

Three of the cards comprise the Disk Control Unit (DCU), two more the Computer Interface Unit (CIU), and eleven other the Analysis Unit (AU). One card slot is reserved for expansion.

2.5.1 Associative Disk File (ADF)

The ADF consists of a 300 megabit Disk Storage Unit with 4 parallel read/write heads and a 16 channel parallel Disk Control Unit.

Disk Storage Unit (DSU)

The DSU is a 3600rpm semi-fixed media moving head disk with 40 recording surfaces and 404 cylinders. Four read/write channels may be connected to any one of ten read/write head groups (4 heads per group). A channel data transfer rate of 1.209 MBytes per second results in a total disk peak data transfer rate of 4.84 MBytes per second.

Each group of 4 recording surfaces is partitioned into six 3072 byte data sectors followed by a 288 byte sector gap. A 4 track parallel sector thus contains a total of 12,288 bytes. A total of 24,240 sectors per spindle provides a total formatted data capacity of 298 million bytes as shown in Figure 2-11.

During a file search, the 4 read/write channels are switched to a new group of read/write heads after each disk revolution. Switching to a new head group (25 microsecond switch time) occurs during a sector gap (197 microseconds). After 10 revolutions, the heads seek a new cylinder. No data is transferred during cylinder seeks, thus reducing the net data transfer rate to 4.02 bytes/microsecond.

Disk Control Unit (DCU)

The DCU interfaces the disk storage unit with the A/P processor and provides for disk head and cylinder selection, the control of read/write operations, and skew/deskew compensation for head alignment variations.

In addition, the DCU transforms 4-channel disk storage unit data into the 16 channel data path which constitutes the disk control unit interface to the A/P processor.

Data blocks, as encoded and formatted by the PDP-11, are stored on the DSU such that two successive data bytes

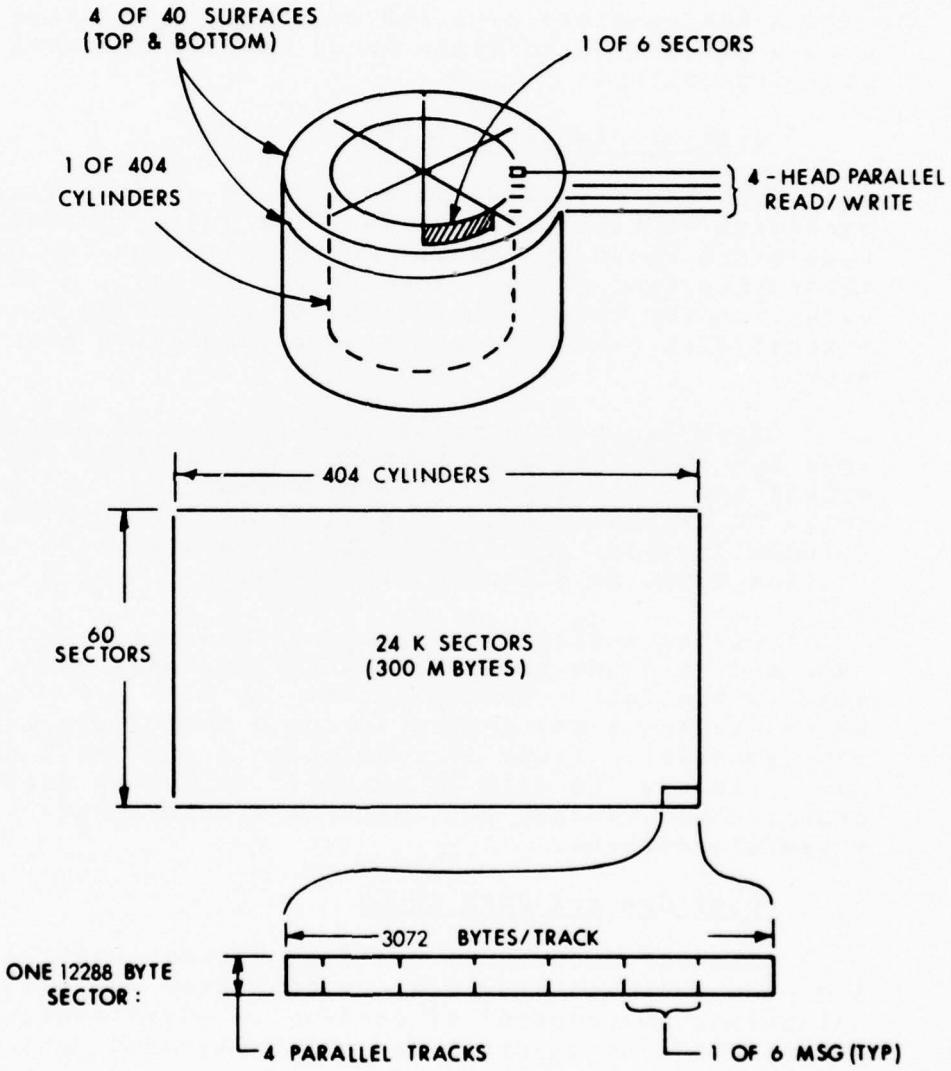


FIGURE 2-11
ADF ORGANIZATION

are stored across 4 tracks of a given cylinder as shown in Figure 2-12.

This data mapping, which provides for hardware minimization in the DCU, is performed entirely by the DCU and is completely transparent to the rest of the system.

2.5.2 Associative Processor

Computer Interface Unit (CIU)

The CIU is the executive of the Associative Processor. This two-card set accepts commands over the UNIBUS, issues commands over an eight bit "Data Vector" Bus to the DCU and AU, conducts data transfers between the UNIBUS and the Data Transfer Bus, and monitors flags from the AU and DCU. The CIU is responsible for maintaining A/P intra-communication, initializing searches, breaking down macro commands from the UNIBUS into a series of micro commands for unit within the A/P, conducting Direct Memory Access (DMA) transfers to PDP-11 Memory, counting the number of messages meeting search criteria, and providing interrupts to the PDP-11.

Analysis Unit (AU)

The AU is an eleven-card set dedicated primarily to conducting searches of the message header and text read from the disk. It also provides buffer space for storing one disk sector of data (6144 sixteen bit words), and buffer space for program information (2048 sixteen bit words). Four of the cards, the Detector Modules are identical. These house the data and program buffer logic to detect the existence of desired words in text, and bipolar storage for the results of the text word detectors. A unique card, the Link Analyzer, performs spatial and logical correlations on the results presented by textword detectors. The six Analysis Control cards coordinate the activity of the other five cards provide data and program buffer address control, respond to commands received over the data vector bus, and present status flags to the CIU. A block diagram of the AU is shown in Figure 2-13.

2.5.3 Data Transfer Bus

The three major units communicate over an internal Data Transfer Bus. Eight lines within the Data Transfer Bus, known as the Data Vector, are driven by the CIU. These lines specify source and destination of a data

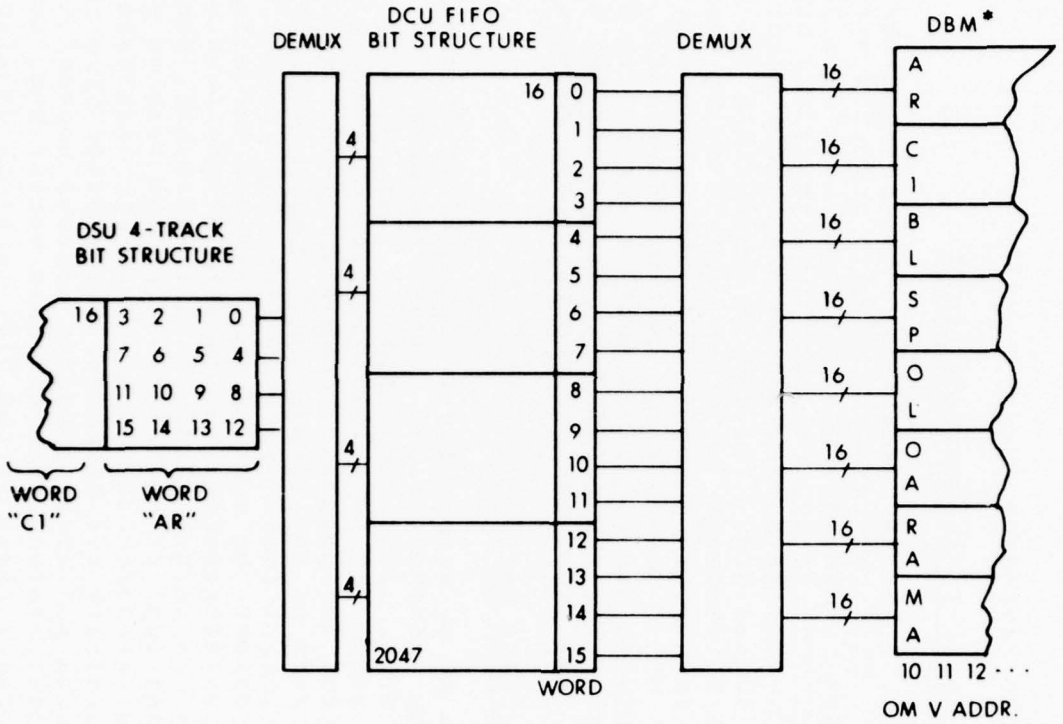


FIGURE 2-12
LOADING DBM FROM DISK

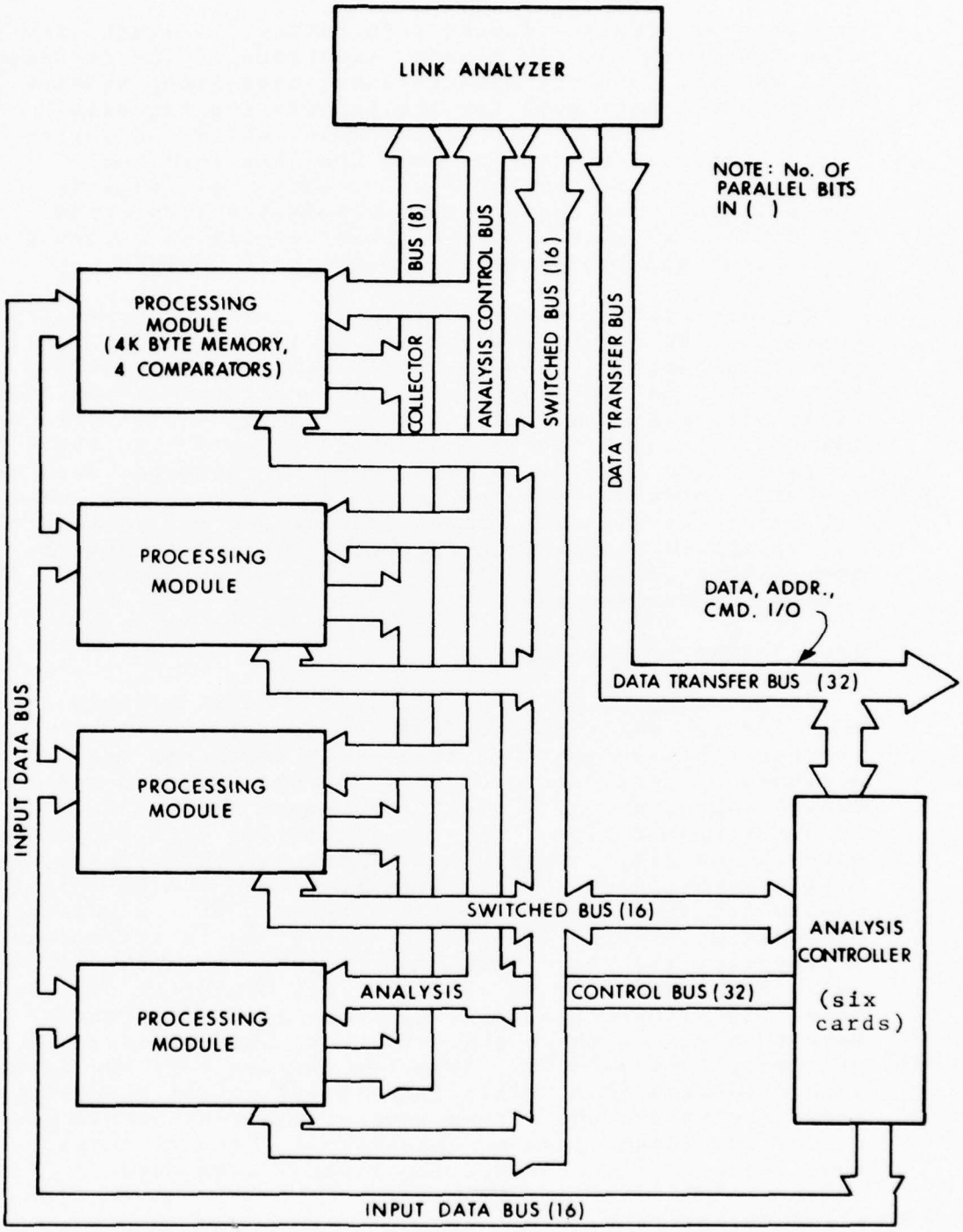


FIGURE 2-13
ANALYSIS UNIT BLOCK DIAGRAM

transfer or provide command information. A ninth line also driven by the CIU causes execution of the deskewed data vector. Sixteen bidirectional data lines provide the internal data path for the Associative Processor and may be driven by any of the major units. A seventeenth line deskews and strobes the data into the location specified by the data vector. The remaining lines in the Data Transfer Bus are status lines from the DCU and AU which indicate error conditions, completion of search, and readiness for additional commands.

To illustrate the use of this bus, take the example where the CIU requests a word of data from the AU. First the CIU places the Data Vector, specifying the desired AU register as the source and a CIU register as destination, onto the Data Vector lines. The execution strobe is issued by the CIU, and the AU raises a busy flag while it looks for the data. The AU places the requested data on the sixteen data lines and pulses the data strobe. The CIU refers to the Data Vector and latches the data into the specified destination register. The AU lowers the busy flag allowing the CIU to issue another command. This closes the transaction.

2.5.4 Free Format Processing

To process the 38.8 megabits per second arriving from the disk in real time requires the use of parallel processing techniques. Sixteen text detectors are arranged in parallel to accomplish this function and are capable of screening: text data, brevity coded data, or a mixture of both. To provide sixteen text detectors with the ability to perform parallel text processing, the disk data buffer memory is organized as a 128 by 768 bit memory (Figure 2-14). The 128 bit width of the memory presents eight bits of data to each of the sixteen text detectors. The eight bits of data could be an ASCII code for a text character or a binary representation of coded data. In either case, literal words generally consist of more than one of these characters or coded fields. It is necessary that each text detector examine only one literal data word at a time. This requirement of the processing array constrains the arrangement of the text within the buffer to sixteen rows of characters. Each of these rows represents one of sixteen literal data words.

2.5.5 Fixed Format Processing

Where brevity coding is used, the multibyte rows constitute an attribute. An attribute, like a literal data word, is a fundamental unit of information. Unlike a

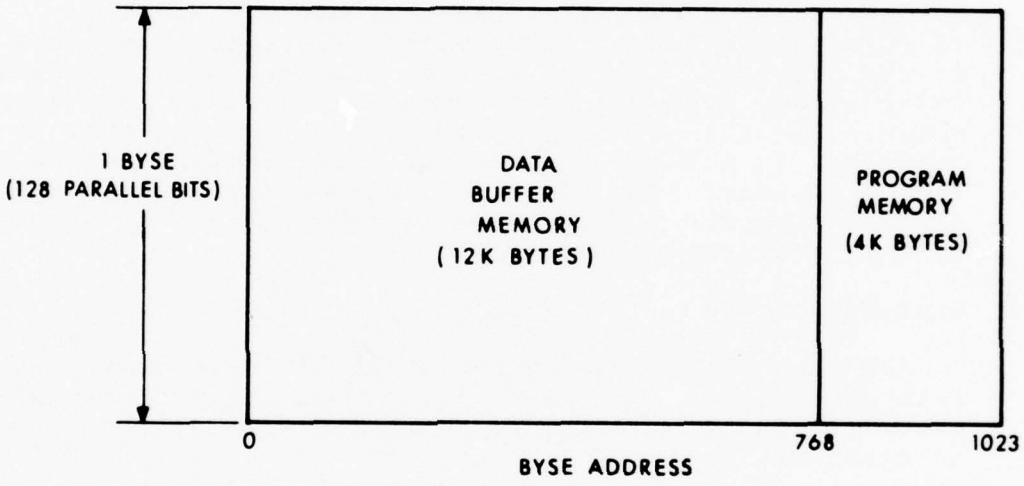


FIGURE 2-14

ORTHOGONAL MEMORY ORGANIZATION

literal data word, an attribute taken out of context has no intrinsic meaning, it is only a number. To derive meaning from an attribute, it is necessary to determine in what type of formatted message the attribute is located. The message format type corresponds to a map of the message indicating where the various types of information are located (e.g., time of day-slice, addressee-slice, originator-slice and so on). Each type of information has a numbered list associated with it (e.g., Ø1-COMASWFORLANT, Ø2-COMSUBLANT, Ø3-COMCARIBSEAFRON). The attribute is the number in the list. If the formatted message had COMCARIBSEAFRON as one of the addressees, the binary representation for Ø3 (00000011) would appear in slice 2 of the message. Clearly without the rest of the positional information, 00000011 would mean very little. Equally obvious are the advantages for using such a scheme. Increases in message information density of 10-100 to one can be realized over free text message information density. As mentioned above, both types of messages may be screened by the Associative Processor.

2.5.6 Disk Data Write

Now that the necessity for a 128 bit wide memory has been established, the unusual disk loading and unloading protocol can be explained. First the disk is commanded to establish markers or headers on each of the 24,240 sector locations indicating the physical address of the sector. Once these information bins have been set up, the data base is created, one sector at a time, as a storage medium to storage medium transfer. Typically, the data base will be sourced and updated from one of the RK05 disk units associated with the PDP-11. Up to 1.2 million 16 bit words can be transferred from such a disk in 6144 16-bit word blocks via the UNIBUS to the Associative Processor. As each of the 16-bit words arrives at the Associative Processor, it is commutated into a 128 bit memory input latch. When eight 16-bit words have been assembled into a 128 bit slice, the resultant slice is written into the disk buffer memory and another slice is assembled in the input latch.

When the 6144 word sector has been written as 768 slices into disk buffer memory, and the sector location to receive the data has been specified, the CIU may be commanded by the PDP-11 to transfer the sector from disk buffer to disk. The CIU, in turn, commands that data transfer to take place over the Data Transfer Bus. A slice is read from the disk buffer into a 128 bit output latch. This slice is read, 16 bits at a time, onto a memory output bus known as the Switched Bus. From there

it is passed by a data path switch, in one of the analysis control cards, to the Data Transfer Bus. The DCU passes the data from the Data Transfer Bus to four 4-bit first-in (FIFO) buffers. The output of each of the four buffers is a 9.7 MHz serial line to each of the four write heads. When the write heads are positioned over the desired sector, the DCU allows data to pass from the FIFOs to the write heads where data is clocked onto the disk. A trailing two byte cyclic redundancy check word is written on the end of the block to provide a means of detecting data errors when the sector is retrieved.

2.5.7 Disk Data Read

Disk data retrieval is accomplished by reversing most of the above steps. Four 9.7 MHz serial lines sourced by the disk read heads input to the four 4-bit FIFOs. The FIFOs output 16 bit deskewed words and the DCU passes these to the Data Transfer Bus. The AU accepts the 16 bit words from the Data Transfer Bus and assembles 128 bit slices in the disk buffer input latch. Slices are written into the disk buffer until the entire sector, 768 slices, have been transferred. Another command moves the contents of the disk buffer output latch, Switched Bus, and Data Transfer Bus. From the UNIBUS and PDP-11 can direct the data to one of its peripherals or a region of memory.

2.5.8 Search-Set Up

Search is a multiple sector read with concurrent text analysis. The disk buffer and program buffer begin the search as empty memories. The program buffer, a 256 x 128 bit memory is loaded first. Program variables include: up to thirty-two literal reference words, relational values between the words, reference character control fields, dimensional information, and search type codes which may be loaded either from the disk or from the UNIBUS. The region of the disk to be searched is specified by the PDP-11 and then a command is issued to begin the search. The DCU seeks the first sector of the search while the Analysis Unit transfers some of the information in the program buffer into bipolar working spaces. When these two tasks have been completed, the CIU sets up a data path between the DCU and the AU, allowing data transfer from the disk to the disk buffer.

2.5.9 Search-Textword Detection

After the data begins to accumulate in the disk buffer, the Analysis Control cards transfer data a slice at a time from the disk buffer to the textword detectors.

A slice is then read from the program buffer. This program slice contains eight program elements each of which is broadcast over the Switched Bus to all 16 textword detectors. The program element consists of an eight bit data field and an eight bit control field. The control field specifies the relationship that is desired between the program data characters and the disk data character. Allowed relationships include: equal (=), not equal ($\neq$), greater than (>), less than (<), greater than or equal ($\geq$), less than or equal ($\leq$), don't care (?), and always false ($\emptyset$). The textword detector records the result of each comparison accumulating one bit for each of the program elements. Results for up to thirty-two program elements can be accommodated in this way. Literal reference words or "key-words" like literal data words from the disk are strings of characters arranged horizontally in memory. Since Program Memory and Disk Buffer Memory have the same width, 128 bits, and half of the program space is taken up with control fields, only eight horizontal character strings can be accommodated in the program space. Keywords are thus blocked in groups of eight literal words. The textword detectors are capable of comparing one literal data word with up to thirty-two keywords (four 8-key blocks).

2.5.10 Textword Detectors-Free and Fixed Format

The first step in textword detection is to load the first characters of 16 data words into the textword detectors. The first character of each of the keywords is sequentially loaded into the detectors and compared with all of the data characters. This process continues until all of the first letters of the keywords have been compared with data. The results of the first-character-to-first-character comparisons determine which of the keys will be called for future comparisons. The second data slice is then loaded into the textword detectors. Then the second characters of these keywords which successfully matched data on the previous comparisons are compared to the new data characters. This comparison process continues until one of two events occurs. One event would be a mismatch between keys and data. In this case the textword detectors are rezeroed and comparison is resumed on the next data block. The other event is a successful match between one or more keywords and data words. In this case the textword detector results are transferred to the link analyzer for correlation.

2.5.11 Textword Detectors; One-on-One

There is one exception to the comparison scheme described above. This was developed for very dense

message formatting where as many as eight independent attributes could be arranged in a single slice. This form of comparison is known as one-on-one. Instead of comparing all key elements to all data elements, the key elements are compared only to the data in a corresponding position in the slice. This templating operation generates an eight bit result which is unconditionally transferred to the link analyzer for correlation.

2.5.12 Key Strike Register

The results of the textword detectors are received by a microprocessor which assembles an entity known as a Key Strike Register(KSR). This 32-bit register represents the accumulated results of the 16 textword detectors over the entire message being searched. At the end of the message this register is presented to the correlator which performs logical associations between elements in the register. The microprocessor assembles each 8-bit section of the register according to the search type employed. One-on-One search, as mentioned above, specifies an unconditional load into the KSR. Fixed format search causes the microprocessor to tally one bit for each attribute. Free text search results are delivered to the microprocessor after each data block having at least one successful keyword to data word match. These results are accumulated in such a way that if the keyword appeared anywhere in the message that result will appear in the KSR.

2.5.13 Correlator

At the end of each message the contents of the KSR are delivered to the correlator. This device examines the relationships between the KSR elements to determine ff the candidate message meets search criteria. The correlator outputs five bits. One bit, the HIT bit, indicates the presence of a desired message. The other four bits are correlation outputs from each eight bit section of the KSR. Associations that may be performed include the following:

AND	- Both keywords linked by this operator must be present.
OR	- One of the two keywords linked by this operator must be present.
EXCLUSIVE OR	- One and only one of the two keywords linked by this operator must be present
NOT	- The keyword linked by this operator must not be present.

NAND - The keywords linked by this operator must not appear in the same message.

NOR - Both of the keywords linked by this operator must be absent.

EXCLUSIVE NOR - The keywords linked by this operator must either be both present or both absent.

The program may use any consistent combination of these operators within a group of eight keywords. The program may also use any consistent combination of the above operators with the group correlation outputs to specify the conditions necessary to obtain a message HIT.

2.5.14 Quote Analyzer

In many instances it is desirable to require that keywords appear in a certain order and/or occur within a given interval. One group of eight keywords may be specified in this way. The Quote Analyzer looks through an eight word sliding window at each candidate message and may be programmed to look for any consistent spatial arrangement of the eight keywords within the eight word window. The Quote Analyzer outputs four independent bits (four independent spatial arrangements) to the correlator. The four quote bits are used in conjunction with the group correlation outputs to obtain a message HIT. To the programmer, this means that not only could he specify that the desired message contains the words SOVIET, TURKISH, GERMAN, SUBMARINES, AND NUCLEAR but also the phrases SOVIET NUCLEAR SUBMARINES and GERMAN NUCLEAR SUBMARINES.

2.5.15 Hit Response

Once a desired message has been located, all search operations cease and the CIU executes a prespecified series of instructions in response to the HIT. This instruction series is specified by the PDP-11 at the beginning of the search. Available responses include:

1. DMA transfer message header to PDP-11 core
2. DMA transfer message location to PDP-11 core
3. DMA transfer message to PDP-11 core
4. DMA transfer KSR to PDP-11 core
5. DMA transfer group correlation and quote bits to PDP-11 core
6. Terminate search
7. Increment HIT counter

2.5.16 Summation

The Associative Processor described above, operating in concert with the PDP-11, is able to screen large data bases on the basis of content. This system is powerful enough to perform complex logical and spatial associations on data arriving at a serial rate of 38.8 megabits per second, yet flexible enough to allow an operator at the graphic terminal to enter data requests in a form approximating natural language. The associative processor is a timely addition to the growing family of data processing devices. With such a device the ever increasing store of information can be more successfully managed.

2.6 System Software

2.6.1 INTRODUCTION

The SCAT system is designed to allow an operator to interactively search and update a large data base in real time. This operation can be broken down into three major functions:

1. System initialization
2. Data input
3. Operator interface

System initialization consists of incorporating the necessary modules into the RSX-11M operating system and initializing the Associative Disk File (ADF). Data input is the process by which input messages are read in (from an RK-05), blocked, and stored on the ADF. The operator interface includes those modules which allow the operator to compose, compile and execute search algorithms, display and update messages, and perform other auxiliary tasks.

2.6.2 System Requirements

The hardware system consists of a PDP-11/45 processor with a Decwriter terminal, 128K bytes of memory, 2 RK-05 disks, and paper tape reader and punch. Connected to that will be the associative processor with a 16K byte buffer and a 300M byte Associative Disk File (ADF). The primary operator terminal for SCAT will be an SA 500 graphic display and keyboard.

The SCAT software will operate as several tasks designed to run under the RSX-11M operating system provided by DEC. Each major function will not execute concurrently but must be initiated from the PDP-11 control terminal (DECwriter). Some additional software is necessary to allow multiple operator terminals and simultaneous execution of the data input and operator interface functions.

2.6.3 General Capabilities

2.6.3.1 System Initialization

The first half of SCAT system initialization consists of performing a system generation (SYSGEN). This process allows the user to optimize his RSX-11M operating system to reflect the hardware configuration and system functions he wishes incorporated. Drivers for all the DEC peripherals, for the SA 500 Graphics Display and for the associative processor are incorporated into the operating system at this time. The second half of

SCAT system initialization consists of initializing the ADF. The entire ADF is filled with blank messages and the ADF directory is updated. Bad sectors are flagged and entered into the bad sector map. This process is performed once for each installation of the SCAT system.

2.6.4 Data Input

Data input consists of reading in messages from an input peripheral, blocking each message, updating system pointers and storing the messages on the ADF. First, a message is read in from the RK-05. The capability also exists to input messages from any logical input device in the system i.e., paper tape. Next, the message is blocked. This reformats the message to optimize the search. Header information is encoded and textual data is compressed during blocking. No information is lost. Next, a disk sector for storing the message is found and various system pointers are updated. Finally, the sector is stored back onto the ADF and the message can now be searched, edited, and updated.

In the standalone mode the function of data input is envisioned to be run as a batch process. However, the data input modules are designed to operate as a background task, allowing real time data input.

2.6.5 Operator interface

The operator interface is the heart of the SCAT system. Designed for flexibility and ease of use, the man-machine interface consists of a command module and various sub-modules initiated by a single keystroke (see Figure 2-15). Each submodule performs a mini-function which allows the operator to perform his task.

As an example of man-machine interaction, suppose he wishes to search the last day's traffic for weather reports. Striking the ENTER ALGORITHM key, a blank search algorithm format is displayed on his screen and the analyst can enter his parameters. Using various function keys he specifies TTY messages from certain sources and certain categories and containing the words WEATHER AND FORECASTING. See Appendix A for a detailed description. Finished with composing an algorithm, the operator exits and strikes the COMPILE key. The displayed source algorithm is then compiled into object form. Assuming no errors need be corrected, the operator can then hit the EXECUTE SEARCH key. A list of retrieval options is now displayed and the analyst specifies the file name to be searched (APRIL 16 etc.) and full text retrieval. The system then searches the area on the ADF associated with the file name and

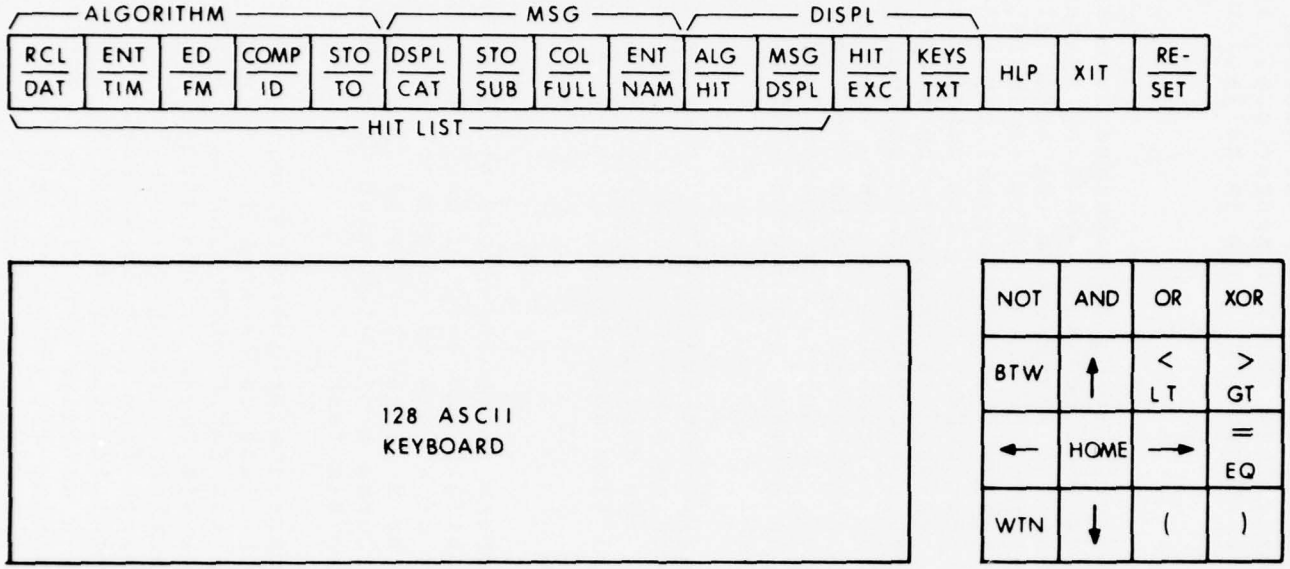


FIGURE 2-15
SA500 SPECIAL FUNCTION KEYS

displays the full text of any message meeting the search criterion. At this point the operator has many options of what to do next. He could select a message, edit it and store it back on the ADF. Another possibility is to recall the search algorithm, re-edit it, re-compile and re-execute. The operator could decide to store the search and execute it later or go on and tackle another problem.

An outline of the single keystroke functions performed by each submodule is given below.

- Retrieve Algorithm

  This key will request an algorithm name as input and will then fetch the named algorithm for execution or edit.

- Enter Algorithm

  This key will blank the screen and initiate the computer assisted algorithm edit routine described below.

- Edit Algorithm

  This key will allow the use of the edit functions on the algorithm currently displayed which may have been entered or retrieved. For a more detailed description of editing search algorithms see Appendix A.

- Compile Algorithm

  This key will compile the currently displayed algorithm which may have been created, edited, or retrieved. The compilation process is described in Appendix A in more detail.

- File Algorithm

  The source of the currently displayed search algorithm will be saved. The name must be provided by the user. If the name is an existing algorithm, it will be replaced, otherwise a new entry in the algorithm file is created.

- Execute Search

  The system will request input of search parameters which are the filename(s) to be searched, and options to be included in the hit list. After these are

entered, a search will be performed by applying the algorithm displayed when the EXECUTE key was struck to the file(s) named.

While the search is in progress, the hit list items specified will be transferred to a buffer until either the search is complete or the buffer is filled. If the buffer is filled before the search is complete, the search will continue but the hit list will be incomplete. A message giving the total number of hits and the number of hits for which information was recorded will be a part of every hit list so that the user may determine if buffer overflow occurred.

The items which are automatically included in each hit list and the optional data which the user can select are:

1. Minimum Information (included by system)

   Message accession number
   ADF sector address (not displayed)
   Message address within sector (not displayed)
   Total number of hits found and recorded

2. Optional Information (may be selected by user)

   Header Information
     Full Header
     Date
     Time
     Source
     Message ID (precedence and security classification)
     Addressee
     Category
     Subcategory
   Full Text
   File name where message was found
   Hit mask that indicates which keys caused the hit

- Display Hit List

  This key will display the list of hits found by the most recently executed search. The hit list will always contain (but not display) the sector address and location of each hit and will always display the accession number of each hit. Optionally, the hit list may display any header attribute, the file name in which the message was found, a hit mask which indentifies keys matched in the message, or the full text of the message.

The user may select one or more messages to be displayed for reading, editing, and/or refiling. If only a few hits on short messages are expected, a useful option is to include the text of the message in the hit list so that the user does not need to read the ADF to get the text.

- Display Message

  If a message was selected from the hit list, it can be read directly using the undisplayed location data in the hit list. If this key is used when a hit list is not displayed, an accession number and optionally a file name must be entered. A search will be executed for the accession number.

  The message will be displayed and the edit functions may be used on the text of the message if desired. If the total message cannot be displayed on the screen, it may be scrolled.

- File Message

  The FILE MESSAGE key may be used while a message is displayed after being retrieved, created, or edited. There are various options available.

  1. Append the edited message to original
  2. Replace the original message in the same file
  3. Copy the message to another file
  4. Copy to another file and delete the original
  5. Delete the original message

- Collect Messages

  The COLLECT key will allow the user to edit and collect portions of the text of several messages into a single message with header and commentary added. The first action in creating such a collection is to create a Message Header and Commentary if desired. Rather than filing this message after its creation, hit the COLLECT key which will put the message into a working file. Then each message from which information is to be copies is called up, all but the desired information is deleted, and the "COLLECT MESSAGE" key is used to add the remaining (undeleted) information to the working file. Upon completion, "EXIT" may be used to call up the working file for further editing or for filing.

- Enter Message

  The ENTER MESSAGE key will blank the screen and allow for the creation of a new header and message using the edit functions.

- Display Keys

  The DISPLAY KEYS key will allow the user to see the keywords that caused a hit. This function will work only if the user has chosen the hit mask as one of the hit list optional parameters and the message was selected from the hit list.

- Exit

  The EXIT key is used to terminate certain interactive operations such as editing or entry of a message or algorithm.

- Reset

  Reset will allow the user to exit from a process during execution. It will terminate both interactive and non-interactive operations. The files which may have been created up to that point will not be saved. After this function is used there can be no recovery.

- Help

  This key will provide information to assist the operator in the use of the system. The "HELP" key may be pressed at any time. It will save the current contents of the display and the cursor position. Information which may be requested by the analyst will include:

  function currently in control
  options currently available
  list of names of filed algorithms
  list of format names
  list of attributes and coded values for each format
  list of file names which may be searched
  list of system functions

  After viewing the information, the analyst may press "EXIT" to return to the status before he requested the help display, or press "RESET" to abort the current function and return to the command module.

Allowing the analyst to specify which functions to perform and in what order makes the operator interface a powerful interactive aid to the operator for solving his data retrieval requirements.

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SECTION 3

SYSTEM HARDWARE

3.1 Major System Components

For the Standalone Configuration, the major system components of the SDCS are:

- CDC 9790 DSU
- PDP-11/45 System Controller with peripherals
- SA 500 Graphics Display System
- A/P Processor

The items and services to be supplied by CDC are listed in Table 3-1 and the items and services to be supplied by DEC are listed in Table 3-2. The item breakdown for the SA 500 Graphics Display System is given in Table 3-3 and the item breakdown for the A/P processor is given in Table 3-4. Piece parts itemization for the A/P Processor is given in Paragraph 3.4.

This section presents a preliminary detailed listing of all major components required to fabricate one Sensor Data Correlation System. Major items with lead times exceeding 90 days are identified. In addition, preliminary parts lists for the 17 wirewrap boards which comprise the SCAT Associative/Parallel Processor and Control Panel are identified.

TABLE 3-1

CDC SUPPLIED ITEMS & SERVICES

QTY	DESCRIPTION	DELIVERY (DAYS)
1	Model 9790 DSU	240
1 Set	Interconnecting Cables	240
1 Set	Operating & Maintenance Manuals	240

TABLE 3-2

DEC SUPPLIED ITEMS & SERVICES

QTY	DESCRIPTION	DELIVERY (DAYS)
1	Central Processor 32K words Parity Memory Memory Management Programmers Console Auto Power Fail/Restart 4 level PAI Hardware Multiply/Divide Cabinet Divide Cabinet Power Supply DEC Writer II & Control	300
1	16K word parity memory & 980 nsec core	300
1	DMA Interface	300
1	Programmable Real Time Clock	300
1	Bootstrap Loader	300
1	High Speed Paper Tape Reader/Punch	300
1	180 CPS Printer	300
1	1.2 meg word disk transport & control for 7 additional transports	300
1	1.2 meg word disk transport	300
1	Peripheral expander panel	300
1	Expansion Cabinet	300
1	RSX11-M on RK disks	300
1	Fortran IV	300

TABLE 3-3

SA 500 ITEMIZATION

QTY	DESCRIPTION	DELIVERY (DAYS ARO)
1	Bootstrap Loader	180
1	Display Generator inc. Digital Display counter, Vector/Position Generator, Stroke Character Generator w/96 ASCII Characters, plus control characters, Dual output display channel, power supply & chassis	180
1	Interface Adapter	180
1	21" Diagonal-High Speed Graphics Indicator (Disk Mounted)	180
1	PHOTOPEN Unit	180
1	Alpha-Numeric Keyboard w/16 Matrix Function Keys and 16 lighted function keys	180
1	PHOTOPEN Intensifier	180
1	Extender Card for 0520 Display Processor PC cards	180

TABLE 3-4

A/P PROCESSOR ITEMIZATION

QTY	DESCRIPTION	DELIVERY (DAYS ARO)
1	Processor Chassis with Control Panel	180
1	Power Supply Chassis	180

3.2 Long Lead Items

All of the items listed in Tables 3-1, 3-2, and 3-3 are long lead items with the stated delivery times as given in the Tables.

3.3 A/P Processor Piece Parts

The A/P Processor is contained in two 10½" high rack mounting assemblies containing a total of 16 component boards, power supplies, and associated hardware. A seventeenth component board is mounted on a swing away Control Panel which fronts one of the two assemblies. An eighteenth card, the unibus interface mounts in the host computer (PDP 11/45). The 18 component boards are identified as follows:

BOARD NO.	DESCRIPTION	QTY
A1A1	DCU Data	1
A1A2	DCU Controller	1
A1A3	DCU Receiver Driver	1
A2A1	CIU Data Card	1
A2A2	CIU Command Card	1
A3A1	AU Detector	4
A3A2	AU Link Analyzer	1
A3A3	Analysis Controller	1
A3A4	Analysis Monitor	1
A3A5	Memory Controller	1
A3A6	Data Address Generator	1
A3A7	Program Address Generator	1
A3A8	Analysis Pilot	1
A4A1	Control Panel Logic	1
A4A2 & A4A3	Mother Board & Card Cage	1
A4A4	Power Supplies (Set of 2)	1
A5A1	Unibus Interface	1

The following pages present a listing of the piece parts contained in the15 board types plus the associated power supplies and other hardware which comprise the Associative Processor.

MATERIAL ESTIMATING SUPPORT

PROPOSAL TITLE	PROPOSAL NO.	RFQ NO.
ASSOCIATIVE PROCESSOR		

ITEM SUB TASK REF.: DISK DATA CONTROLLER

PREPARED BY	DATE	ORG. NO.	ORGANIZATION NAME	APPROVED BY	DATE
C. WOOD	3/14/77	1-2350			

LINE #	REFERENCE NUMBER	PART NUMBER	DWG. REV.	PART DESCRIPTION	SOURCE	PRICING BASE CAT.	BID.	EST.	QTY.	UNIT PRICE	TOTAL PRICE	DELIV.
1		SN7400N		2 input nand gate	TIPA+MIN 5.00				3	.14		
2		SN74S02N		2 input nor gate	"				5	.20		
3		SN7404N		inverter	"				5	.15		
4		SN74S04N		inverter	"				1	.22		
5		SN74S10N		3 input nand gate	"				2	.20		
6		SN74S11N		3 input and gate	"				2	.20		
7		SN7420N		4 input nand gate	"				2	.14		
8		SN74S20N		4 input nand gate	"				4	.20		
9		SN74H21N		4 input and gate	"				3	.17		
10		SN7427N		3 input nor gate	"				2	.17		
11		SN7432N		2 input or gate	"				1	.17		
12		SN74S74N		flip flop	"				4	.28		
13		SN74109N		flip flop	"				3	.30		
14		SN74LS112N		flip flop	"				1	.30		
15		SN74153N		multiplexer	"				1	.40		
16		SN74S153N		multiplexer	"				2	.72		
17		SN74S157N		multiplexer	"				4	.73		
18		SN74S158N		multiplexer	"				2	.42		

MATERIAL ESTIMATING SUPPORT

PROPOSAL TITLE	PROPOSAL NO.	RFQ NO.
ASSOCIATIVE PROCESSOR		

ITEM SUB TASK REF.
DISK DATA CONTROLLER

PREPARED BY	DATE	ORG. NO.	ORGANIZATION NAME	APPROVED BY	DATE
C. WOOD	3/14/77	1-2350			

LINE #	REFERENCE NUMBER	PART NUMBER	DWG. REV.	PART DESCRIPTION	SOURCE	PRICING BASE CAT.	BID.	EST.	QTY.	UNIT PRICE	TOTAL PRICE	DELIV.
19		SN74162N		Counter	TIPA+MIN 5.00				1	2.94		
20		SN74163N		Counter	"				4	.47		
21		SN74179N		Register	"				4	3.29		
22		SN74LS241N		3-state driver	"				1	1.45		
23		SN74276N		flip flop	"				6	..66		
24		SN74S374N		register	"				2	3.25		
25		N825100-1		PLA	Signetics				1	37.50		
26		AM25LS161PC		Counter	AMD				13	1.56		
27		67401		FIFO	MMI				4	25.00		
28		102-14-AA-B		14 pin WW socket	Garry				39	1.06		
29		102-16-AA-B		16 pin WW socket	Garry				39	1.12		
30		102-20-AA-B		20 pin WW socket	Garry				9	1.56		
31		300-28-AA-B		28 pin WW socket	Garry				1	2.49		
32		102-14-FF-B		14 pin header	Garry				1	1.10		
33		RCR07G102J3		1KΩ¼W resistor					2	.04		
34		CK05BX104K		.1μf @50V capacitor					32	.81		
35		F9401PC		CRC generator	Fairchild				4	10.56		
36		150D107X9025S2		100μf @20V capacitor	Sprague				1	4.38		

BOARD: A1A1

MATERIAL ESTIMATING SUPPORT

PROPOSAL TITLE: ASSOCIATIVE PROCESSOR | PROPOSAL NO. | RFQ NO.

ITEM/SUB TASK REF.: DISK DATA CONTROLLER

PREPARED BY: C. WOOD | DATE: 3/14/77 | ORG NO.: 1-2350 | ORGANIZATION NAME | APPROVED BY | DATE

ITEM	REFERENCE NUMBER	PART NUMBER	DWG. REV.	PART DESCRIPTION	SOURCE	PRICING BASE: CAT.	BID.	ESC.	QTY.	UNIT PRICE	TOTAL PRICE	DELIV.
27		7011935P001		Inductor	SA				1	.26		
28		583243-8		160 p/n connector	AMP				1	27.33		
29		6942 Rev A		Wire Wrap Board	SA				1			

BOARD: A1A1

MATERIAL ESTIMATING SUPPORT

PROPOSAL TITLE	PROPOSAL NO.	RFQ NO.
ASSOCIATIVE PROCESSOR		

ITEM SUB TASK REF.: DISK COMMAND CONTROLLER

PREPARED BY	DATE	ORG. NO	ORGANIZATION NAME	APPROVED BY	DATE
C. WOOD	3/14/77	1-2350			

LINE #	REFERENCE NUMBER	PART NUMBER	DWG. REV.	PART DESCRIPTION	SOURCE	PRICING BASE CAT.	BID.	EST.	QTY.	UNIT PRICE	TOTAL PRICE	DELIV.
1		SN7400N		2 input nand gate	TIPA+MIN 5.00				1	.14		
2		SN74S00N		2 input nand gate	"				1	.20		
3		SN7402N		2 input nor gate	"				1	.14		
4		SN7403N		2 input nand gate	"				1	.14		
5		SN7404N		inverter	"				3	.15		
6		SN74S04N		inverter	"				1	.22		
7		SN7408N		2 input and gate	"				1	.14		
8		SN74S10N		3 input nand gate	"				1	.20		
9		SN74S32N		2 input or gate	"				3	.28		
10		Sn7485N		4 bit comparator	"				1	4.19		
11		SN74109N		flip flop	"				1	.30		
12		SN74138N		1 of 8 decoder	"				1	.48		
13		SN74139N		1 of 4 decoder	"				1	.86		
14		SN74LS153N		multiplexer	"				7	.40		
15		SN74LS157N		multiplexer	"				3	.42		
16		SN74174N		register	"				6	.58		
17		SN74195N		register	"				3	.38		
18		SN74LS241N		3-state driver	"				2	1.45		

BOARD: A1A2

MATERIAL ESTIMATING SUPPORT

BOARD: A1A2

PROPOSAL TITLE	PROPOSAL NO.	REQ NO.
ASSOCIATIVE PROCESSOR		

ITEM OR TASK REF.
DISK COMMAND CONTROLLER

PREPARED BY	DATE	ORG. NO.	ORGANIZATION NAME	APPROVED BY	DATE
E. Wood	3/14/77	1-2350			

ITEM NO.	REFERENCE NUMBER	PART NUMBER	DWG. REV.	PART DESCRIPTION	SOURCE	PRICING BASE CAT.	BID.	EST.	QTY.	UNIT PRICE	TOTAL PRICE	DELIV.
19		SN74251N		multiplexer	TIPA+MIN 5.00				3	.47		
20		SN74276N		flip flop	TIPA+MIN 5.00				1	.66		
21		SN74S374N		register	TI				7	3.25		
22		AM2901DC		microprocessor	AMD				4	42.00		
23		6301		PROM	MMI				1	2.00		
24		6306		PROM	MMI				11	4.60		
25		67110		UCU	MMI				1	21.50		
26		AM2913DC		RAM	AMD				4	36.00		
27		102-14-TF-B		14 pin header	Garry				1	1.10		
28		102-14-AA-B		14 pin WW socket	Garry				15	1.06		
29		102-16-AA-B		16 pin WW socket	Garry				37	1.12		
30		102-20-AA-B		20 pin WW socket	Garry				9	1.56		
31		400-22-AA-B		22 pin WW socket	Garry				4	1.56		
32		300-40-AA-B		40 pin WW socket	Garry				5	3.86		
33		RCR07G512J3		5.1KΩ¼W resistor					2	.04		
34		RCR07G471J3		470Ω¼W resistor					1	.04		
35		RCR076102J3		1KΩ¼W resistor					1	.04		
36		CK05BX104J		.1MF 050V capacitor					20	.81		

MATERIAL ESTIMATING SUPPORT

PROPOSAL TITLE	PROPOSAL NO.	RFQ NO.
ASSOCIATIVE PROCESSOR		

ITEM, SUB TASK REF.
DISK COMMAND CONTROLLER

PREPARED BY	DATE	ORG. NO.	ORGANIZATION NAME	APPROVED BY	DATE
C. Wood	3/14/77	1-2350			

ITEM NO.	REFERENCE NUMBER	PART NUMBER	DWG. REV.	PART DESCRIPTION	SOURCE	PRICING BASE CAT.	BID.	EST.	QTY.	UNIT PRICE	TOTAL PRICE	DELIV.
37		552245-8		160 pin connector	AMP				1	27.33		
38		150D107X9025S2		100 f @20V capacitor	Sprague				1	4.38		
39		7019358001		Inductor	SA				1	.26		
40		6962 Rev A		Wire Wrap Board	SA				1			

BOARD: A1A2

MATERIAL ESTIMATING SUPPORT

PROPOSAL TITLE	PROPOSAL NO.	RFQ NO.
ASSOCIATIVE PROCESSOR		

ITEM/SUB TASK REF.: DISK REC/DRIVER

PREPARED BY	DATE	ORG NO.	ORGANIZATION NAME	APPROVED BY	DATE
C. WOOD	3/14/77	1-2350			

LINE #	REFERENCE NUMBER	PART NUMBER	DWG. REV.	PART DESCRIPTION	SOURCE	PRICING BASE CAT.	BID.	EST.	QTY.	UNIT PRICE	TOTAL PRICE	DELIV.
1		SN7402N		2 input nor gate	TIPA+MIN 5.00				1	.14		
2		SN7404N		inverter	"				1	.15		
3		SN74S113N		flip flop	"				2	.36		
4		SN74LS241N		3-state driver	"				1	1.45		
5		DS3650		receiver	National				4	5.85		
6		SN75110		driver	TI				15	.91		
7		4116R-002-221		220Ωresistor network	Bourns				4	1.20		
8		4116R-002-471		47Ωresistor network	Bourns				2	1.20		
9		4116R-002-102		1KΩresistor network	Bourns				1	1.20		
10		4116R-002-682		6.8KΩresistor network	Bourns				1	1.20		
11		102-14-AA-B		14 pin WW socket	Garry				19	1.06		
12		102-16-AA-B		16 pin WW socket	Garry				12	1.12		
13		102-20-AA-B		20 pin WW socket	Garry				1	1.56		
14		583245-8		160 pin connector	AMP				1	27.33		
15		7011935P001		inductor	SA				1	.26		
16		CK05BX104K		.1μf @50V capacitor					15	.81		
17		150D107X9025 2		100μf @20V capacitor	Spraque				1	4.38		
18		6942 Rev A		Wire Wrap Board	SA				1			

BOARD: A1A3

MATERIAL ESTIMATING SUPPORT

PROPOSAL TITLE	PROPOSAL NO.	RFQ NO.
ASSOCIATIVE PROCESSOR		

ITEM SUB TASK REF.
CIU DATA

PREPARED BY	DATE	ORG. NO.	ORGANIZATION NAME	APPROVED BY	DATE
C. WOOD	3/14/77	1-2350			

LINE #	REFERENCE NUMBER	PART NUMBER	DWG. REV.	PART DESCRIPTION	SOURCE	PRICING BASE CAT.	BID.	EST.	QTY.	UNIT PRICE	TOTAL PRICE	DELIV.
1		SN7400N		2 input nand gate	TIPA+MIN 5.00				6	.14		
2		SN7402N		2 input nor gate	"				1	.14		
3		SN7404N		inverter	"				3	.15		
4		SN7408N		2 input and gate	"				2	.14		
5		SN7410N		3 input nand gate	"				2	.14		
6		SN74LS14N		Schmitt-trigger inverter	"				1	.89		
7		SN7420N		4 input nand gate	"				2	.14		
8		SN7425N		4 input nor gate	"				1	.14		
9		SN7427N		3 input nor gate	"				2	.17		
10		SN7432N		2 input or gate	"				1	.17		
11		SN7451N		and-or-invert gate	"				1	.14		
12		SN7474N		flip flop	"				1	.21		
13		SN74148N		priority encoder	"				2	.60		
14		SN74157N		multiplexer	"				1	.40		
15		SN74LS169N		counter	"				4	3.60		
16		SN74175N		register	"				2	.50		
17		SN74S189N		RAM	"				4	6.96		
18		SN74LS240N		3-state driver	"				2	1.06		

BOARD: A2A1

MATERIAL ESTIMATING SUPPORT

PROPOSAL TITLE	PROPOSAL NO.	RFQ NO.
ASSOCIATIVE PROCESSOR		

ITEM SUB TASK REF.: CIU DATA

PREPARED BY	DATE	ORG. NO.	ORGANIZATION NAME	APPROVED BY	DATE
C. WOOD	3/12/77	1-2350			

LINE #	REFERENCE NUMBER	PART NUMBER	DWG. REV.	PART DESCRIPTION	SOURCE	PRICING BASE CAT.	BID.	EST.	QTY.	UNIT PRICE	TOTAL PRICE	DELIV.
19		SN74S240N		3-state driver	TIPA+MIN 5.00				1	2.57		
20		SN74LS241N		3-state driver	"				17	1.45		
21		SN74265N		comp output element	"				1	.39		
22		SN74276N		Flip Flop	"				1	.66		
23		SN74S374N		Register	"				2	3.25		
24		AM25LS161PC		counter	AMD				9	1.56		
25		A1414 10.0MHz		osc	M.F. Electronics				1	53.00		
26		67401		FIFO	MMI				4	25.00		
27		102-14-AA-B		14 pin WW Socket	Garry				25	1.06		
28		102-16-AA-B		16 pin WW Socket	Garry				29	1.12		
29		102-20-AA-B		20 pin WW Socket	Garry				23	1.56		
30		102-14-FF-B		14 pin header	Garry				1	1.10		
31		RCR07G102J3		1KΩ ¼W resistor					2	.04		
32		1N4148		Diode					1	.03		
33		M39003/01-2254		4.7μf@10V capacitor	SA				1	.20		
34		CK05BX104J		.1μf@50V capacitor					20	.81		
35		105D107x902S2		100μf@20V capacitor	Sprague				1	4.38		
36		7011935P001		inductor	SA				1	.26		

MATERIAL ESTIMATING SUPPORT

BOARD: A2A1

PROPOSAL TITLE	PROPOSAL NO.	RFQ NO.
ASSOCIATIVE PROCESSOR		

ITEM SUB TASK REF.

CIU DATA

PREPARED BY	DATE	ORG. NO.	ORGANIZATION NAME	APPROVED BY	DATE

ITEM NO.	REFERENCE NUMBER	PART NUMBER	DWG. REV.	PART DESCRIPTION	SOURCE	PRICING BASE CAT.	BID.	EST.	QTY.	UNIT PRICE	TOTAL PRICE	DELIV.
37		6101		PROM	MMI				2	2.00		
38		583345-8		160 pin connector	AMP				1	27.33		
22		6342 Rev A		Wire Wrap Board	SA				1			

MATERIAL ESTIMATING SUPPORT

PROPOSAL TITLE	PROPOSAL NO.	RFQ NO.
ASSOCIATIVE PROCESSOR		

WBS SUB TASK REF.
CIU CONTROL

PREPARED BY	DATE	ORG. NO.	ORGANIZATION NAME	APPROVED BY	DATE
G. Todd	3/14/77	1-2350			

ITEM	REFERENCE NUMBER	PART NUMBER	CHG. REV.	PART DESCRIPTION	SOURCE	PRICING BASE CAT.	BID.	EST.	QTY.	UNIT PRICE	TOTAL PRICE	DELIV.
1		SN7400N		2 input nand gate	TIPA+MIN 5.00				5	.14		
2		SN74S00N		2 input nand gate	"				1	.20		
3		SN7402N		2 input nor gate	"				4	.14		
4		SN7403N		2 input nand gate	"				1	.14		
5		SN7404N		inverter	"				3	.15		
6		SN74S04N		inverter	"				2	.22		
7		SN7408N		2 input and gate	"				4	.14		
8		SN74S08N		2 input and gate	"				1	.20		
9		SN7410N		3 input nand gate	"				2	.14		
10		SN74LS21N		4 input and gate	"				1	.20		
11		SN7425N		4 input nor gate	"				1	.14		
12		SN7427N		3 input nor gate	"				4	.17		
13		SN74S32N		2 input or gate	"				1	.28		
14		SN7451N		and-or-invert gate	"				1	.14		
15		SN7474N		Flip Flop	"				2	.21		
16		SN7486N		2 input exclusive gate	"				1	.21		
17		SN74109N		Flip Flop	"				2	.30		
18		SN74148N		Priority encoder	"				2	.60		

AD-A041 330 SANDERS ASSOCIATES INC NASHUA N H F/G 15/4
SENSOR DATA CORRELATION SYSTEM DEVELOPMENT (DESIGN PHASE).(U)
JUN 77 J L BURROWS, T MOORE, B ROSSIN F30602-76-C-0341
UNCLASSIFIED SAN-GA-77-110-2 RADC-TR-77-191 NL

2 OF 2
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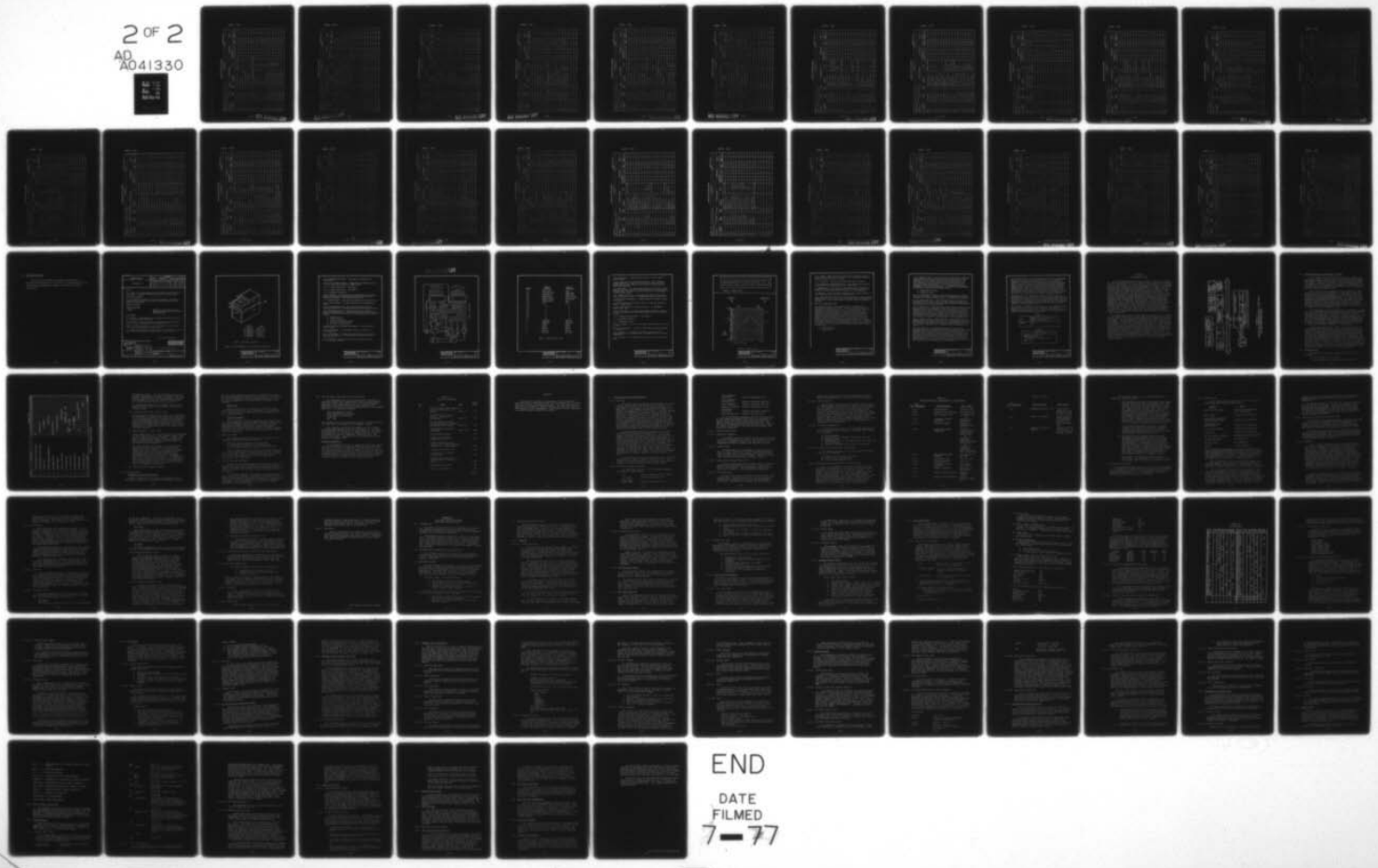
A041330



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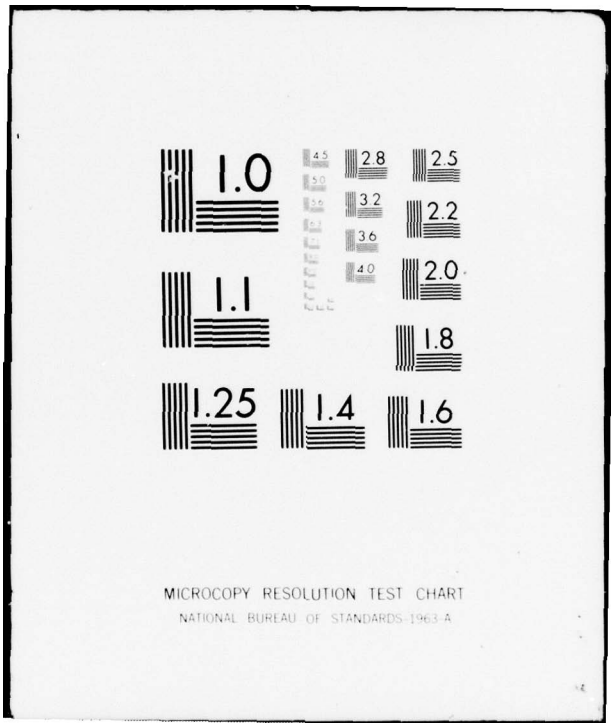
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MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

MATERIAL ESTIMATING SUPPORT

PROPOSAL TITLE	PROPOSAL NO.	RFQ NO.
ASSOCIATIVE PROCESSOR		

ITEM SUB TASK REF.
CIU CONTROL

PREPARED BY	DATE	ORG. NO.	ORGANIZATION NAME	APPROVED BY	DATE
C. WOOD	3/14/77	1-2350			

LINE #	REFERENCE NUMBER	PART NUMBER	DWG. REV.	PART DESCRIPTION	SOURCE	PRICING BASE CAT.	BID.	EST.	QTY.	UNIT PRICE	TOTAL PRICE	DELIV.
19		SN74151N		Multiplexer	TIPA+MIN 5.00				1	.41		
20		SN74175N		register	"				3	.50		
21		SN74S175N		register	"				1	3.25		
22		SN74180N		parity generator	"				1	3.61		
23		SN74LS241N		3-state driver	"				7	1.45		
24		SN74LS243N		3-state driver	TI				9	2.67		
25		SN74259N		8 bit addressable latch	TIPA+MIN 5.00				1	1.07		
26		SN74S374N		register	TI				1	3.25		
27		AM25S07PC		register	AMD				2	1.56		
28		6301		PROM	MMI				7	2.00		
29		6331		PROM	MMI				1	1.60		
30		TID136N		diode terminator	TI				7	3.75		
31		102-14-AA-B		14 pin WW Socket	GARRY				51	1.05		
32		102-16-AA-B		16 pin WW Socket	GARRY				20	1.12		
33		102-20-AA-B		20 pin WW Socket	GARRY				8	1.56		
34		102-14-FF-B		14 pin header	GARRY				1	1.10		
35		RCR07651253		5.1K 1/4W resistor					2	.04		
36		RCR07691153		910 1/4W resistor					2	.04		

BOARD: A2A2

MATERIAL ESTIMATING SUPPORT

PROPOSAL TITLE	PROPOSAL NO.	RFQ NO.
ASSOCIATIVE PROCESSOR		

ITEM SUB TASK REF.
CIU CONTROL

PREPARED BY	DATE	OPC NO.	ORGANIZATION NAME	APPROVED BY	DATE
C. WOOD	3/14/77	1-2350			

BOARD: A2A2

ITEM	REFERENCE NUMBER	PART NUMBER	DWG. REV.	PART DESCRIPTION	SOURCE	PRICING BASE CAT.	PRICING BASE BID.	PRICING BASE EST.	QTY.	UNIT PRICE	TOTAL PRICE	DELIV.
37		RCR07G102J3		1KΩ,W resistor					1	.04		
38		CK05BX104J		.1uf @50V capacitor					20	.81		
39		150K107X9025S2		100uf @20V capacitor	Sprague				1	4.38		
40		7011035P001		inductor	SA				1	.26		
41		583245-3		160 pin connector	AMP				1	27.33		
42		3432-3005		40 pin Scotchplex header	3M				2	5.76		
43		6943 Rev A		Wire Wrap Board	SA				1			

MATERIAL ESTIMATING SUPPORT

PROPOSAL TITLE: ASSOCIATIVE PROCESSOR | PROPOSAL NO. | REQ NO.

ITEM SUB TASK REQ.: A F DETECTOR

PREPARED BY: C. Todd | DATE: 3/14/77 | ORG NO.: 1-2350 | ORGANIZATION NAME | APPROVED BY | DATE

LEVEL	REFERENCE NUMBER	PART NO. DRP	DRG. DIV.	PART DESCRIPTION	SOURCE	PRICING BASE CAT.	BID.	EST.	QTY.	UNIT PRICE	TOTAL PRICE	DELIV.
1		SN74S04N		Inverter	TIPA+MIN 5.00				1	.22		
2		SN74S09N		2 input and gate	"				4	.93		
3		SN74S32N		2 input or gate	"				4	.28		
4		SN74S85N		4 bit comparator	TI				8	9.17		
5		SN74151AN		multiplexer	TIPA+MIN 5.00				4	.41		
6		SN74S175N		register	"				5	.50		
7		SN74LS240N		3-state driver	"				1	2.77		
8		SN74S241N		3-state driver	"				1	2.57		
9		SN74LS241N		3-state driver	"				5	1.45		
10		SN74LS299N		register	"				16	5.00		
11		SN74S374N		register	"				12	3.25		
12		AM25LS163PC		counter	AMD				1	1.56		
13		4104AGP		RAM	Lmm Semi				8	22.40		
14		DS0026CN		clock driver	National				1	5.85		
15		LM320T-6		5V voltage regulator	National				1	4.15		
16		102-8-AA-B		8 pin WW socket	Garry				2	.75		
17		102-14-AA-B		14 pin WW socket	Garry				9	1.06		
18		102-16-AA-B		16 pin WW socket	Garry				19	1.12		

BOARD: A3A1

MATERIAL ESTIMATING SUPPORT

PROPOSAL TITLE	PROPOSAL NO.	RFQ NO.
ASSOCIATIVE PROCESSOR		

ITEM SUB TASK REF.
AP DETECTOR

PREPARED BY	DATE	ORG. NO.	ORGANIZATION NAME	APPROVED BY	DATE
C. WOOD	3/14/77	1-2350			

LINE	REFERENCE NUMBER	PART NUMBER	DWG. REV.	PART DESCRIPTION	SOURCE	PRICING BASE CAT.	BID.	EST.	QTY.	UNIT PRICE	TOTAL PRICE	DELIV.
19		102-20-AA-B		20 pin WW socket	Garry				35	1.56		
20		400-22-AA-B		22 pin WW socket	Garry				8	1.56		
21		300-24-AA-B		24 pin WW socket	Garry				1	1.95		
22		102-8-FF-B		8 pin header	Garry				1	.75		
23		300-24-FF-B		24 pin header	Garry				1	1.91		
24		1N4606		Diode					2	1.32		
25		936D156X0020SQ		capacitor network	Sprague				1			
26		RCR07G100J3		10Ω 1W resistor					1	.04		
27		CKR05BX681M		680pf capacitor					1	.09		
28		150D107X002S2		100uf @20V capacitor	Sprague				3	4.38		
29		CK05BX104K		.1uf @50V capacitor					56	.81		
30		70119357001		inductor	SA				3	.26		
31		583245-3		160 pin connector	AMP				1	27.33		
32		6942 Rev A		wire wrap board	SA				1			

MATERIAL ESTIMATING SUPPORT

PROPOSAL TITLE	PROPOSAL NO.	RFQ NO.
ASSOCIATIVE PROCESSOR		

ITEM SUB TASK REF.
LINK ANALYZER

PREPARED BY	DATE	ORG. NO.	ORGANIZATION NAME	APPROVED BY	DATE
C. WOOD	3/14/77	1-2350			

LINE #	REFERENCE NUMBER	PART NUMBER	DWG. REV.	PART DESCRIPTION	SOURCE	PRICING BASE CAT.	BID.	EST.	QTY.	UNIT PRICE	TOTAL PRICE	DELIV.
1		SN74S08N		2 input and gate	TIPA+MIN 5.00				4	.20		
2		SN74S138N		1 of 8 decoder	"				2	.86		
3		SN74148N		priority encoder	"				1	.60		
4		SN74S189N		RAM	"				9	6.96		
5		SN74LS240N		3-state driver	"				3	1.06		
6		SN74LS241N		3-state driver	TI				2	1.45		
7		SN74LS244N		3-state driver	TI				1	2.77		
8		SN74376N		flip flop	TIPA+MIN 5.00				1	.35		
9		SN74LS377N		register	TI				1	2.74		
10		AM25LS161PC		counter	AMD				28	1.56		
11		AM27LS00PC		RAM	AMD				9	5.00		
12		150D107X902S2		100μf @ 20V capacitor	Sprague				1	4.38		
13		CK05BX104K		.1μf @ 50V capacitor					62	.81		
14		7011935P001		inductor	SA				1	.26		
16		102-8-AA-B		8 pin WW socket	Garry				1	.65		
17		102-14-AA-B		14 pin WW socket	Garry				4	1.06		
18		102-16-AA-B		16 pin WW socket	Garry				50	1.12		

BOARD: A3A2

MATERIAL ESTIMATING SUPPORT

BOARD: A3A2

PROPOSAL TITLE	PROPOSAL NO.	RFQ NO.
ASSOCIATIVE PROCESSOR		

ITEM SUB TASK REF.
LINE ANALYZER

PREPARED BY	DATE	ORG. NO.	ORGANIZATION NAME	APPROVED BY	DATE
C. WOOD	3/14/77	1-2350			

ITEM NO.	REFERENCE NUMBER	PART NUMBER	DWG. REV.	PART DESCRIPTION	SOURCE	PRICING BASE CAT.	BID.	EST.	QTY.	UNIT PRICE	TOTAL PRICE	DELIV.
19		102-20-AA-8		20 pin WW socket	Garry				7	1.56		
20		102-8-FF-8		8 pin header	Garry				1	.75		
21		RCR07G102J3		1K ¼W resistor					1	.04		
22		150D107X9025S2		100 f @20V capacitor	Sprague				1	4.38		
23		CK05BX104K		.1 f @50V capacitor					62	.81		
24		7011935P001		inductor	SA				1	.26		
25		583245-8		160 pin connector	AMP				1	27.33		
26		6942 Rev A		Wire Wrap Board	SA				1			

MATERIAL ESTIMATING SUPPORT

PROPOSAL TITLE	PROPOSAL NO.	RFQ NO.
ASSOCIATIVE PROCESSOR		

ITEM SUB TASK REF. ANALYSIS CONTROLLER

PREPARED BY	DATE	ORG. NO.	ORGANIZATION NAME	APPROVED BY	DATE

LINE #	REFERENCE NUMBER	PART NUMBER	DWG. REV.	PART DESCRIPTION	SOURCE	PRICING BASE CAT.	BID.	EST.	QTY.	UNIT PRICE	TOTAL PRICE	DELIV.
1		SN74LS244N		Octal Tristate Buffer	TI				4	2.77		
2		SN74LS240N		Octal Tristate Buffer	TI PA+$5.00 MIN				4	1.06		
3		SN74S374N		Octal Tristate Latch	TIPA +$5.00 MIN				6	3.25		
4		AM25S18PC		4 Bit Tristate Latch	AMD				4	3.00		
5		6331		32 x 8 PROM	MMI				5	2.00		
6		SN74S05N		Hex Open Collector Driver	TIPA +$5.00 MIN				1	.22		
7		SN74S32N		Quad Positive or Gate	"				5	.28		
8		SN74S157N		Quad Two input MUX	"				3	.75		
9		SN74LS157N		Quad Two Input MUX	"				2	.67		
10		93427PC		256 x 4 PROM	FAIRCHILD PA				1	2.50		
11		SN74S189N		16 x 4 RAM	TI				1	6.86		
12		SN74LS259N		8 bit Addressable Latch	TI PA+$5.00 MIN				1	1.07		
13		SN74376N		Quad JK Flip Flop	"				1	.35		
14		SN74S08N		Quad Positive and gate	"				1	.20		
15		SN74109N		Dual JK Flip Flop	"				3	.30		
16		SN74LS30N		8 input nand gate	"				1	.17		
17		AM25LS163PC		4 bit synchronous counter	AMD				4	1.56		
18		SN74S153N		Dual 4 to 1 MUX	TI PA+$5.00 MIN				1	.72		

BOARD: A3A3

MATERIAL ESTIMATING SUPPORT

PROPOSAL TITLE	PROPOSAL NO.	RFQ NO.
ASSOCIATIVE PROCESSOR		

ITEM/SUB TASK REF.
ANAYSIS CONTROLLER

PREPARED BY	DATE	ORG. NO.	ORGANIZATION NAME	APPROVED BY	DATE

LINE #	REFERENCE NUMBER	PART NUMBER	DWG. REV.	PART DESCRIPTION	SOURCE	PRICING BASE			QTY.	UNIT PRICE	TOTAL PRICE	DELIV.
						CAT.	BID.	EST.				
19		SN74151AN		8 input MUX	TIPA+$5.00 MIN				1	.41		
20		SN74S10N		Triple 3 input Nand Gate	"				2	.20		
21		SN74S04N		Hex Inverter	"				2	.22		
22		SN74LS139N		Dual 2 to 4 Demux	"				1	.86		
23		SN74LS02N		Quad 2 input nor gate	"				2	.19		
24		SN74S74N		Dual D flip flop	"				3	.28		
25		SN74LS299N		Tristate Shift Register	TI			X	2	5.00		
26		SN74LS379N		4 bit gated Latch	TIPA+$5.00 MIN				1	3.26		
27		DM85S68N		16 x 4 register File	NATIONAL				2	6.82		
28		SN74S20N		Dual 4 input nand gate	TIPA+$5.00 MIN				1	.20		
29		SN74S02N		Quad Two input nor gate	TIPA+$5.00 MIN				1	.20		
30		102-14-AA-B		14 pin WW socket	GARRY				19	1.06		
31		102-16-AA-B		16 pin WW socket	GARRY				29	1.12		
32		102-18-AA-B		18 pin WW socket	GARRY				2	1.48		
33		102-20-AA-B		20 pin WW socket	GARRY				16	1.56		
34		CK05BX104J		0.1uf 50V Cap	SPRAGUE				66	.81		
35		150D107X90S2		100uf 20V Cap	SPRAGUE				1	4.38		
36		7011935P001		Toroid Inductor	SA				1	.26		

BOARD: A3A3

MATERIAL ESTIMATING SUPPORT

PAGE 3 OF 3

PROPOSAL TITLE	PROPOSAL NO.	RFQ NO.
ASSOCIATIVE PROCESSOR		

ITEM SUB TASK REF.
ANALYSIS CONTROLLER

PREPARED BY	DATE	ORG. NO.	ORGANIZATION NAME	APPROVED BY	DATE

LINE #	REFERENCE NUMBER	PART NUMBER	DWG. REV.	PART DESCRIPTION	SOURCE	PRICING BASE CAT.	BID.	EST.	QTY.	UNIT PRICE	TOTAL PRICE	DELIV.
37		583245-8		160 pin Connector	AMP				1	27.33		
38		6942REVA		Wire Wrap Board	S/A				1	--		
39		914C102X5PE		Resistor Network	SPRAGUE				1	1.24		

BOARD: A3A3

MATERIAL ESTIMATING SUPPORT

PROPOSAL TITLE	PROPOSAL NO.	RFQ NO.
ASSOCIATIVE PROCESSOR		

ITEM SUB TASK REF.
ANALYSIS MONITOR

PREPARED BY	DATE	ORG. NO.	ORGANIZATION NAME	APPROVED BY	DATE

LINE #	REFERENCE NUMBER	PART NUMBER	DWG. REV.	PART DESCRIPTION	SOURCE	PRICING BASE CAT.	BID.	EST.	QTY.	UNIT PRICE	TOTAL PRICE	DELIV.
1		SN74LS244N		Octal Tristate Buffer	TI				4	2.77		
2		SN74LS374N		Octal Tristate Latch	TI				2	3.25		
3		SN74LS241N		Octal Tristate Buffer	TIPA+$5.00 MIN				2	1.06		
4		SN74LS240N		Octal Tristate Buffer	TIPA+$5.00 MIN				2	1.06		
5		SN74S374		Octal Tristate Latch	TIPA + 20%				5	3.25		
6		6331		32 x 8 PROM	MMI				5	2.00		
7		93427PC		256 x 4 PROM	FAIRCHILD PA				8	2.50		
8		AM25LS163PC		4 bit synchronous counter	AMD				7	1.56		
9		SN74S151N		8 input MUX	TI				1	.41		
10		SN74376N		Quad JK Flip Flop	TIPA+$5.00 MIN				2	.35		
11		SN74S132N		Quad Schmitt Trigger Nand	TI				1	.28		
12		SN74S20N		Dual 4 input nand gate	TIPA+5.00 MIN				1	.20		
13		SN74S09N		Quad Open Collector and gate	"				1	.93		
14		SN74S74N		Dual D Flip Flop	"				1	.28		
15		SN74S158N		Quad Two input Mux-Inverting	"				2	.42		
16		SN74S00N		Quad Two input nand gate	"				2	.20		
17		SN74S02N		Quad Two input nor gate	"				1	.20		
18		SN74109N		Dual JK Flip Flop	"				1	.30		

MATERIAL ESTIMATING SUPPORT

PROPOSAL TITLE	PROPOSAL NO.	RFQ NO.
ASSOCIATIVE PROCESSOR		

ITEM SUB TASK REF.
ANALYSIS MONITOR

PREPARED BY	DATE	ORG. NO.	ORGANIZATION NAME	APPROVED BY	DATE

LINE #	REFERENCE NUMBER	PART NUMBER	DWG. REV.	PART DESCRIPTION	SOURCE	PRICING BASE CAT.	BID.	EST.	QTY.	UNIT PRICE	TOTAL PRICE	DELIV.
19		SN74S08N		Quad Two input and gate	TIPA+$5.00 MIN				3	.20		
20		SN74S04N		HEX Inverter	"				2	.22		
21		SN74S32N		Quad Two input or gate	"				1	.28		
22		914C102X5PE		Resistor Network	SPRAGUE				1	1.24		
23		102-14-AA-B		14 pin WW Socket	GARRY				14	1.06		
24		102-16-AA-B		16 pin WW socket	GARRY				26	1.12		
25		102-20-AA-B		20 pin WW socket	GARRY				15	1.56		
26		CK05BX104J		0.1uf 50V Cap	SPRAGUE				55	.81		
27		150D107X90S2		100uf 20V cap	SPRAGUE				1	4.38		
28		7011935P001		Toroid Inductor	S/A				1	.26		
29		583245-8		160 pin connector	AMP				1	27.33		
30		6942REVA		Wire Wrap Board	S/A				1	---		

BOARD: A3A4

3/29/3-30

MATERIAL ESTIMATING SUPPORT

BOARD: A3A5

PROPOSAL TITLE	PROPOSAL NO.	RFQ NO.
ASSOCIATIVE PROCESSOR		

ITEM SUB TASK REF.
MEMORY CONTROLLER

PREPARED BY	DATE	SRC NO.	ORGANIZATION NAME	APPROVED BY	DATE
J. WOOD	5/31/77	1-2350			

ITEM	REFERENCE NUMBER	PART NUMBER	DWG. REV.	PART DESCRIPTION	SOURCE	PRICING BASE CAT.	BID	EST.	QTY.	UNIT PRICE	TOTAL PRICE	DELIV.
1		74LS00N		2 input nand gate	TIPA+MIN 5.00				1	.19		
2		74LS02N		2 input nor gate	"				1	.19		
3		74S04N		inverter	"				1	.22		
4		74S05N		inverter	"				1	.22		
5		74S10N		3 input nand gate	"				1	.20		
6		74S20N		4 input nand gate	"				1	.20		
7		74S30N		8 input nand gate	"				1	.22		
8		74S32N		2 input or gate	"				1	.28		
9		74S74N		flip flop	"				1	.28		
10		74S132N		2 input nand gate	"				1	.48		
11		74S138N		1of8 decoder	"				1	.86		
12		74148N		priority encoder	"				1	.60		
13		75S157N		multiplexer	"				1	.73		
14		74LS240N		3-state driver	"				2	2.77		
15		74LS244N		3-state driver	TI				1	2.77		
16		74265N		comp output element	TIPA+MIN 5.00				1	.39		
17		74LS299N		register	"				2	.66		
18		74S174N		register	"				2	3.29		

MATERIAL ESTIMATING SUPPORT

PROPOSAL TITLE: ASSOCIATIVE PROCESSOR | PROPOSAL NO. | RFQ NO.

NEW SUB TASK REF.: MEMORY CONTROLLER

PREPARED BY: C. WOOD | DATE: 3/2/77 | ORG. NO.: 1-2350 | ORGANIZATION NAME | APPROVED BY | DATE

ITEM NO.	REFERENCE NUMBER	PART NUMBER	ENG. REV.	PART DESCRIPTION	SOURCE	PRICING BASE CAT.	BID.	EST.	QTY.	UNIT PRICE	TOTAL PRICE	DELIV.
19		AM25LS161PC		counter	AMD				1	1.56		
20		AM25LS163PC		counter	AMD				1	1.56		
21		6331		PROM	MMI				2	2.00		
22		102-14-AA-3		14pin WW socket	GARRY				10	1.06		
23		102-16-AA-3		16 pin WW socket	GARRY				8	1.12		
24		102-20-AA-3		20 pin WW socket	GARRY				7	1.56		
25		70F1335P001		Inductor	SA				1	.26		
26		150D107X90252		100uf @20V capacitor	SPRAQUE				1	4.33		
27		CK05BX104K		.1uf @50V capacitor					24	.31		
28		583245-8		160 pin connector	AMP				1	27.33		

MATERIAL ESTIMATING SUPPORT

BOARD: A3A6

PROPOSAL TITLE		PROPOSAL NO.	RFQ NO.
ASSOCIATIVE PROCESSOR			
ITEM/SUB TASK REF.			
DATA ADDRESS GENERATOR			
PREPARED BY	DATE	ORG. NO.	ORGANIZATION NAME / APPROVED BY / DATE
C. WOOD	4/5/77	1-2350	

LINE #	REFERENCE NUMBER	PART NUMBER	DWG. REV.	PART DESCRIPTION	SOURCE	PRICING BASE CAT.	BID.	EST.	QTY.	UNIT PRICE	TOTAL PRICE	DELIV.
1		74LS04N		inverters	TIPA + MIN 5.00				1	.22		
2		74S08N		2 input and gate	TIPA + MIN 5.00				2	.20		
3		74S10N		3 input nand gate	TIPA + MIN 5.00				1	.20		
4		74LS10N		3 input nand gate	TIPA + MIN 5.00				1	.20		
5		74S32N		2 input or gate	TIPA + MIN 5.00				4	.28		
6		74LS74N		flip flop	TIPA + Min 5.00				1	.30		
7		74LS85N		comparator	TI				3	9.17		
8		74S138N		decoder	TIPA + MIN 5.00				1	.86		
9		74151AN		multiplexer	TIPA + MIN 5.00				1	.41		
10		74S157N		multiplexer	TIPA + MIN 5.00				1	.73		
11		74S158N		multiplexer	TIPA + MIN 5.00				1	.42		
12		74LS164N		register	TIPA + MIN 5.00				1	1.35		
13		74LS174N		register	TIPA + MIN 5.00				2	.81		
14		74LS175N		register	TIPA + MIN 5.00				1	.75		
15		74LS240N		3-state driver	TIPA + MIN 5.00				1	1.06		
16		74LS244N		3-state driver	TIPA + MIN 5.00				7	2.77		
17		74LS283N		full adder	TIPA + MIN 5.00				4	1.89		
18		74S374N		register	TIPA + MIN 5.00				2	1.89		

MATERIAL ESTIMATING SUPPORT

BOARD: A3A6

PROPOSAL TITLE	PROPOSAL NO.	RFQ NO.
ASSOCIATIVE PROCESSOR		

ITEM/SUB TASK REF.
DATA ADDRESS GENERATOR

PREPARED BY	DATE	ORG. NO.	ORGANIZATION NAME	APPROVED BY	DATE
C. WOOD	4/6/77	1-2350			

LINE #	REFERENCE NUMBER	PART NUMBER	DWG. REV.	PART DESCRIPTION	SOURCE	PRICING BASE			QTY.	UNIT PRICE	TOTAL PRICE	DELIV.
						CAT.	BID.	EST.				
19		74LS378N		register	TIPA+MIN 5.00				2	2.03		
20		74LS379N		register	"				1	3.26		
21		74LS670N		register file	"				3	1.48		
22		AM25LS163PC		counter	AMD				10	1.56		
23		6301		PROM	MMI				4	2.00		
24		6331		PROM	MMI				5	2.00		
25		DM8160		comparator	NATIONAL				4	4.00		
26		93L422		RAM	FAIRCHILD	X			3	44.00		
27		102-8-AA-B		8 pin WW socket	GARRY				1	.65		
28		102-14-AA-B		14 pin WW socket	GARRY				10	1.06		
29		102-16-AA-B		16 pin WW socket	GARRY				44	1.12		
30		102-20-AA-B		20 pin WW socket	GARRY				10	1.56		
31		600-22-AA-B		22 pin WW socket	GARRY				3	1.56		
32		102-8FF-B		8 pin header	GARRY				1	.75		
33		7011935P001		inductor	SA				1	.26		
34		RCR07G102J3		1KΩ¼W resistor					2	.04		
35		105D107X902S2		100uf @20V capacitor	SPRAQUE				1	4.38		
36		CK05BX104K		.1uf @50V capacitor					63	.81		

MATERIAL ESTIMATING SUPPORT

PROJECT TITLE		PROPOSAL NO.	REQ NO.
ASSOCIATIVE PROCESSOR			
ITEM SUB TASK PCP.			
DATA ADDRESS GENERATOR			

PREPARED BY	DATE	ECC NO.	ORGANIZATION NAME	APPROVED BY	DATE
G. FROD	10/6/77	1-2350			

W.S.	REFERENCE NUMBER	PART NUMBER	ENG. REV	PART DESCRIPTION	SOURCE	PRICING BASE CAT.	PRICING BASE BID.	PRICING BASE EST.	QTY.	UNIT PRICE	TOTAL PRICE	DELIV.
27		583243-8		160 pin connector	AMP				1	27.33		

BOARD: A3A6

MATERIAL ESTIMATING SUPPORT

PROPOSAL TITLE	PROPOSAL NO.	RFQ NO.
ASSOCIATIVE PROCESSOR		

ITEM SUB TASK REF.

PROGRAM ADDRESS GENERATOR

PREPARED BY	DATE	ORG NO.	ORGANIZATION NAME	APPROVED BY	DATE
C. WOOD	3/31/77	1-2350			

ITEM NO.	REFERENCE NUMBER	PART NUMBER	DWG. REV.	PART DESCRIPTION	SOURCE	PRICING BASE CAT.	BID.	EST.	QTY.	UNIT PRICE	TOTAL PRICE	DELIV.
1		74S02N		2 input nor gate	TIPA+MIN 5.00				1	.20		
2		74S00N		2 input and gate	"				2	.20		
3		74S20N		4 input nand gate	"				1	.20		
4		74LS20N		4 input nand gate	"				1	.17		
5		74LS27N		3 input nor gate	"				1	.20		
6		74LS30N		8 input nand gate	"				1	.19		
7		74S32N		2 input or gate	"				3	.28		
8		74LS32N		2 input or gate	"				3	.18		
9		74LS109N		flip flop	"				3	.23		
10		74S138N		1 of 8 decoder	"				1	.86		
11		74LS174N		register	"				1	.70		
12		74S175N		register	"				1	.50		
13		74LS244N		3-state driver	TI				3	2.77		
14		74LS259N		8 bit addressable latch	TIPA+MIN 5.00				2	1.07		
15		74LS283N		full adder	"				2	1.89		
16		74LS299N		register	"				3	.66		
17		74S374		register	"				1	1.07		
18		74LS378		register	"				3	2.03		

BOARD: A3A7

MATERIAL ESTIMATING SUPPORT

PROPOSAL TITLE		PROPOSAL NO.	REQ NO.
ASSOCIATIVE PROCESSOR			
WORK UNIT TASK REF.			
PROGRAM ADDRESS GENERATOR			
PREPARED BY	DATE	ORG. NO.	ORGANIZATION NAME
C. WOOD	3/31/77	1-2350	
APPROVED BY		DATE	

ITEM NO.	REFERENCE NUMBER	PART NUMBER	DRG. REV.	PART DESCRIPTION	SOURCE	PRICING BASE CAT.	BID.	EST.	QTY.	UNIT PRICE	TOTAL PRICE	DELIV.
19		74LS670		register bite					6	1.48		
20		6301		PROM					1	2.00		
21		DM8160		6 bit comparator					2	4.00		
22		AM2S68		RAM					2	6.82		
23		AM25LS161PC		counter					2	1.56		
24		102-8-AA-B		8 pin WW socket					1	.65		
25		102-14-AA-B		14 pin WW socket					13	1.06		
26		102-16-AA-B		16 pin WW socket					24	1.12		
27		102-18-AA-B		18 pin WW socket					2	1.48		
28		102-20-AA-B		20 pin WW socket					7	1.56		
29		102-8-TF-B		8 pin header					1	.75		
30		RCR07G102J3		1KΩ¼W resistor					1	.04		
31		70119350001		inductor					1	.26		
32		150D107X9025S2		100uf @20V capacitor					1	4.38		
33		CK05BX104K		.1uf @50V capacitor					45	.81		
34		583245-8		100 pin connector					1	27.33		

MATERIAL ESTIMATING SUPPORT

PROPOSAL TITLE	PROPOSAL NO.	RFQ NO.
ASSOCIATIVE PROCESSOR		

ITEM/SUB TASK REF.
ANALYSIS PILOT

PREPARED BY	DATE	ORG. NO.	ORGANIZATION NAME	APPROVED BY	DATE

LINE #	REFERENCE NUMBER	PART NUMBER	DWG. REV.	PART DESCRIPTION	SOURCE	PRICING BASE			QTY.	UNIT PRICE	TOTAL PRICE	DELIV.
						CAT.	BID.	EST.				
1		SN74S74N		Dual D Flip Flop	TIPA +$5.00MIN				1	.28		
2		SN74S08N		Quad Two input and gate	"				2	.20		
3		SN74S158N		Quad Two input Mux - inverting	"				1	.42		
4		SN74S10N		Triple three input nand gate	"				2	.20		
5		SN74109N		Dual JK Flip Flop	"				4	.30		
6		SN74148N		8 bit priority encoder	"				1	.60		
7		SN74S32N		Quad two input or gate	"				3	.28		
8		AM25LS163PC		synchronous 4 bit counter	AMD				2	1.56		
9		914C102X5PE		resistor network	SPRAGUE				1	1.24		
10		SN74376N		Quad JK Flip Flop	TIPA +$5.00MIN				1	.35		
11		SN74S11N		Triple 3 input and gate	"				1	.20		
12		SN74S02N		Quad two input nor gate	"				1	.20		
13		SN74S00N		Quad two input nand gate	"				1	.20		
14		SN74S04N		Hex inverter	"				2	.22		
15		93427PC		256 x 4 Prom	FAIRCHILD PA				3	2.50		
16		DM8136N		6 bit bus comparator	NATIONAL				1	4.00		
17		SN74LS377N		Octal gated latch	TI				1	2.74		
18		SN74LS244N		Octal tristate buffer	TI				2	2.77		

BOARD: A3A8

MATERIAL ESTIMATING SUPPORT

PROPOSAL TITLE	PROPOSAL NO.	RFQ NO.
ASSOCIATIVE PROCESSOR		

ITEM/SUB TASK REF.
ANALYSIS PILOT

PREPARED BY	DATE	ORG. NO.	ORGANIZATION NAME	APPROVED BY	DATE

LINE #	REFERENCE NUMBER	PART NUMBER	DWG. REV.	PART DESCRIPTION	SOURCE	PRICING BASE CAT.	BID.	EST.	QTY.	UNIT PRICE	TOTAL PRICE	DELIV.
19		SN74LS240N		Octal Tristate Buffer	TIPA +$5.00 MIN				2	1.06		
20		SN74S374N		Octal Tristate Latch	"				3	3.25		
21		SN74195N		4 bit shift register	"				1	.38		
22		102-14-AA-B		14 pin WW socket	GARRY				15	1.06		
23		102-16-AA-B		16 pin WW socket	GARRY				14	1.12		
24		102-20-AA-B		20 pin WW socket	GARRY				8	1.56		
25		CK05BX104J		0.1uf 50V cap	SPRAGUE				36	.81		
26		150D107X90S2		100uf 20V cap	SPRAGUE				1	4.38		
27		7011935P001		Toroid Inductor	S/A				1	.26		
28		583245-8		160 pin connector	AMP				1	27.33		
29		6942REVA		Wire Wrap Board	S/A				1	---		
30		SN74S20N		Dual 4 input nand gate	TIPA +$5.00MIN				1	.20		

BOARD: A3A8

MATERIAL ESTIMATING SUPPORT

PROPOSAL TITLE	PROPOSAL NO.	RFQ NO.
ASSOCIATIVE PROCESSOR		
ITEM/SUB TASK REF. AP CONTROL PANEL		

PREPARED BY	DATE	ORG NO.	ORGANIZATION NAME	APPROVED BY	DATE
C. WOOD	5/14/77	1-2350			

ITEM NO.	REFERENCE NUMBER	PART NUMBER	DWG. REV.	PART DESCRIPTION	SOURCE	PRICING BASE CAT.	BID.	EST.	QTY.	UNIT PRICE	TOTAL PRICE	DELIV.
1		SN74LS00N		2 input nand gate	MIPA+MIN 5.00				3	.19		
2		SN74LS02N		2 input nor gate	"				2	.19		
3		SN74LS04N		inverter	"				3	.20		
4		SN74LS08N		2 input and gate	"				2	.19		
5		SN74LS11N		3 input and gate	"				1	.20		
6		SN74LS14N		Schmitt-trigger inverter	"				1	.89		
7		SN74LS20N		4 input nand gate	"				1	.17		
8		SN74LS21N		4 input and gate	"				1	.20		
9		SN74LS27N		3 input nor gate	"				1	.20		
10		SN74LS30N		8 input nand gate	"				2	.19		
11		SN74LS32N		2 input or gate	"				1	.18		
12		SN74LS86N		2 input exclusive or gate	"				2	.34		
13		SN74LS123N		Monostable Multivibrate	"				2	.60		
14		SN74148N		priority encoder	"				4	.60		
15		SN74LS154N		1 of 16 decoder	"				1	.78		
16		SN74LS157N		Multiplexer	"				5	.67		
17		SN74LS174N		register	"				3	.70		
18		SN74LS241N		3-state driver	"				6	1.45		

BOARD: A4A1

MATERIAL ESTIMATING SUPPORT

PROPOSAL TITLE	PROPOSAL NO.	RFQ NO.
ASSOCIATIVE PROCESSOR		

ITEM SUB TASK REF.
AP CONTROL PANEL

PREPARED BY	DATE	ORG. NO.	ORGANIZATION NAME	APPROVED BY	DATE
C. WOOD	3/14/77	1-2350			

BOARD: A4A1

LINE #	REFERENCE NUMBER	PART NUMBER	DWG. REV.	PART DESCRIPTION	SOURCE	PRICING BASE CAT.	BID.	EST.	QTY.	UNIT PRICE	TOTAL PRICE	DELIV.
19		SN74LS243N		3-state driver	TI				1	2.67		
20		SN74LS279N		S-R latch	TIPA+MIN 5.00				1	.37		
21		SN74LS298N		Multiplexer with storage	"				4	.66		
22		SN74376N		register	"				2	.35		
23		25LS161PC		counter	AMD				5	1.56		
24		TID136N		Diode Terminator	TI				7	3.75		
25		N82S100-1		PLA	Signetics				1	37.50		
26		75452		High current driver					4	.41		
27		4116R-002-512		5.1K resistor network	Bourns				2	1.20		
28		102-14-AA-B		14 pin WW Socket	Garry				37	1.06		
29		102-16-AA-B		16 pin WW Socket	Garry				35	1.12		
30		102-20-AA-B		20 pin WW Socket	Garry				6	1.56		
31		300-24-AA-B		24 pin WW Socket	Garry				1	1.95		
32		300-28-AA-B		28 pin WW Socket	Garry				1	2.49		
33		102-16-FF-B		16 pin header	Garry				2	1.27		
34		RCR07G512J3		5.1KΩ¼ resistor					3	.04		
35		RCR07G363J3		36KΩ¼W resistor					2	.04		
36		RCR07G103J3		10KΩ¼W resistor					2	.04		

MATERIAL ESTIMATING SUPPORT

BOARD: A4A1

PROPOSAL TITLE	PROPOSAL NO.	REQ NO.
ASSOCIATIVE PROCESSOR		

ITEM WBS TASK REF.
AP CONTROL PANEL

PREPARED BY	DATE	ORG NO.	ORGANIZATION NAME	APPROVED BY	DATE
C. Wood	3/14/77	1-2350			

ITEM NO.	REFERENCE NUMBER	PART NUMBER	DWG. REV.	PART DESCRIPTION	SOURCE	PRICING BASE CAT.	BID.	EST.	QTY.	UNIT PRICE	TOTAL PRICE	DELIV.
37		RCR07G102J3		1KΩ¼W resistor					1	.04		
38		1N4148		diode					1	.03		
39		CM06FD102JP3		1KPf capacitor					2	.20		
40		M39003/01-2259		33μf @10V capacitor					1	.26		
41		WMF05P18		.18μf @50V capacitor	CDE				2	.45		
42		CK05BX104K		.1μf @50V capacitor					16	.81		
43		3432-3005		40 pin Scotchflex header	3M				2	5.76		
44		3429-3005		26 pin Scotchflex header	3M				3	4.30		
45		150D107X9025S2		100μf @20V capacitor	Sprague				1	4.38		
46		7011935P001		inductor	SA				1	.26		
47		6942 Rev B		Wire Wrap Board	SA				1			
48		745-0007		Hex Display	Railco				9			
49		965-1ZJ6		Hex Keyboard	Cherry				2			

(3-44 thru 3-46 are left blank)

MATERIAL ESTIMATING SUPPORT

BOARD: A4A3

PROPOSAL TITLE	PROPOSAL NO.	RFQ NO.
ASSOCIATIVE PROCESSOR		

ITEM/SUB TASK REF.
CARD FILE & EXTENDER BOARD

PREPARED BY	DATE	ORG. NO.	ORGANIZATION NAME	APPROVED BY	DATE
C. Wood	10/15/77	1-2350			

NO.	REFERENCE NUMBER	PART NUMBER	DWG. REV.	PART DESCRIPTION	SOURCE	PRICING BASE CAT.	E.D.	EST.	QTY.	UNIT PRICE	TOTAL PRICE	DELIV.
1		583245-8		160 pin connector	AMP				1	27.33		
2		583247-9		160 pin connector	AMP				1	31.48		
3		3-583292-5		160 pin connector	AMP				15	29.93		
4		89714		Mother Board	SA				2			
5		60032		Card Guide	OPL Scanble				2	10.84		
6		60049		End Plate	OPL Scanble				2	3.84		
7	SA#	105052661		Card Guide	CAR Prod				1	33.00		
8	SA#	105052662		Card Guide	CAR Prod				1	33.00		
9		4575-M210		Extender Board	SA				1			

MATERIAL ESTIMATING SUPPORT

PROPOSAL TITLE	PROPOSAL NO.	RFQ NO.
ASSOCIATIVE PROCESSOR		

ITEM SUB TASK REF.
POWER SUPPLIES

PREPARED BY	DATE	ORG. NO.	ORGANIZATION NAME	APPROVED BY	DATE
C. WOOD	3/14/77	1-2350			

LINE #	REFERENCE NUMBER	PART NUMBER	DWG. REV.	PART DESCRIPTION	SOURCE	PRICING BASE CAT.	BID.	EST.	QTY.	UNIT PRICE	TOTAL PRICE	DELIV.
1		HCC512		-5,+12V Power Supply	Powerone Inc.				1	86.95		
2		CF-5-J/100A		+5V Power Supply	Power Mate Corp.				1	435.00		

BOARD: A4A4

MATERIAL ESTIMATING SUPPORT

BOARD: A5A1

PROPOSAL TITLE	PROPOSAL NO.	RFQ NO.
ASSOCIATIVE PROCESSOR		

ITEM SUB TASK REF.
UNIBUS INTERFACE

PREPARED BY	DATE	ORG. NO.	ORGANIZATION NAME	APPROVED BY	DATE
C. WOOD	5/14/77	1-2350			

ITEM NO.	REFERENCE NUMBER	PART NUMBER	DWG. REV.	PART DESCRIPTION	SOURCE	PRICING BASE CAT.	BID.	EST.	QTY.	UNIT PRICE	TOTAL PRICE	DELIV.
1		N82S100-1		PLA	Signetics				1	37.50		
2		DS8641		Unibus driver/receiver	National				12	2.75		
3		DS8640		Unibus receiver	National				1	1.25		
4		SN74LS241N		3-state driver	TIPA+MIN 5.00				13	1.45		
5		SN74LS386J		3-state driver	TI				1	2.75		
6		TID136N		diode terminator	TI				7	3.75		
7		102-16-FF-B		16 pin header	Garry				1	1.27		
8		RCR07G102J3		1KΩ¼W resistor					2	.04		
9		RCR07G181J3		180Ω¼W resistor					2	.04		
10		RCR07G391J3		390Ω¼W resistor					2	.04		
11		RCR07G511J3		510Ω¼W resistor					2	.04		
12		3432-3005		40 pin Scotchflex header	3M				2	5.76		
13		C1P-4-32-30		DEC interface board	Garry				1	235.00		
14		150D107X9025S2		100uf @20V capacitor	Sprague				1	4.38		
15		CK05BX104J		.1μf @50V capacitor					26	.81		
16		7011935P001		Inductor	SA				1	.26		

3.4 DSU Specification

This section contains the Sanders Associates, Inc. purchase specification to be used for the procurement of the Control Data Corporation's Model No. 9790 Disk Storage Unit (DSU).

SOURCE(S) OF SUPPLY	REVISIONS				
	LTR	REFERENCE	DATE	APVD	APVD
SEE TABLE II	—	DEVELOPMENT RELEASE	[illegible]	[illegible]	[illegible]

1. SCOPE

1.1 Scope.- This specification covers the detail requirements for a data storage disk memory intended for use with the SCAT16 System.

2. APPLICABLE DOCUMENTS

2.1 The following documents of the issue in effect on the date of invitation for bids shall form a part of this specification to the extent specified herein.

OTHER PUBLICATIONS

Control Data Corp.

Manual	Equipment Specification for disk Storage Unit BR304 Customer Engineering Manual BK304

3. REQUIREMENTS

3.1 General.- Units supplied to this specification shall conform to the requirements specified herein.

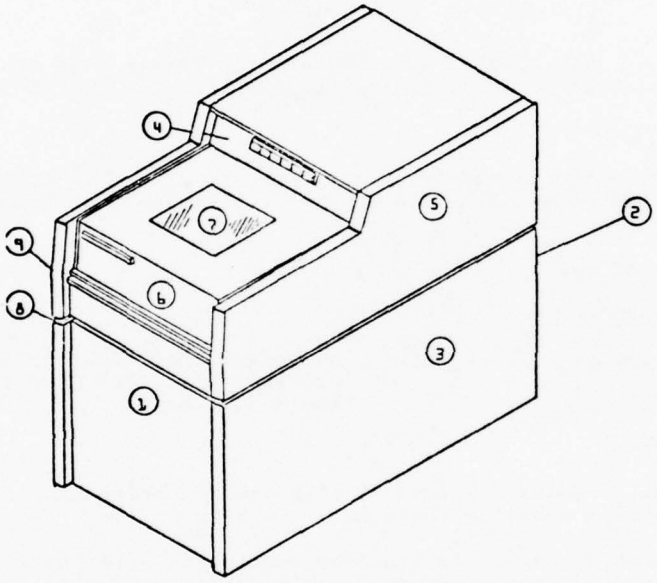
3.2 Materials.- Materials shall be used which will enable the disk memory to meet the requirements of this specification.

3.2.1 Printed Circuit Boards.- All printed circuit board material shall be a flame retardant glass epoxy laminate.

3.3 Design and Construction.- Units shall be of the design, construction, and physical dimensions specified herein, (See Figure 1).

SPECIFICATION CONTROL

THIS DOCUMENT IS ISSUED IN THE SANDERS SPECIFICATION & STD SYSTEM. THE FORMAT IS IN ACCORDANCE WITH SA-STD-251.			PROCUREMENT SPECIFICATION	
	PREPARED	—	—	
	CHECKED	[illegible]	[illegible]	DISK MEMORY, DATA STORAGE
	ENGINEER	[illegible]	[illegible]	
	PROJECT	—	—	CODE IDENT NO 94117 / SPECIFICATION NO 8 0 0 1 9 5
	RLSE/CONT			
				SHEET 1 OF



	ASSEMBLY	COLOR
1.	FRONT DOOR	IMPERIAL BLUE
2.	REAR COVER	IMPERIAL BLUE
3.	SIDE PANEL	LIGHT GRAY
4.	CONTROL PANEL	IMPERIAL BLUE
5.	TOP COVER	LIGHT GRAY
6.	PACK ACCESS	IMPERIAL BLUE
7.	COVER GLASS	LIGHT BLUE
8.	BELTLINE	GRAY BLACK
9.	TRIM STRIP	IMPERIAL BLUE

FIGURE 1. DISK STORAGE UNIT BR3D8-A

Note: Physical Dimension to be Supplied at a later date.

PROCUREMENT SPECIFICATION	SPECIFICATION NO 8 0 0 1 9 5	REV —
	CODE IDENT NO 94117	SHEET 2

3.3.1 Connectors and Cables.- See Table I for connector pin designations.

3.3.1.1 A.C. Power Connector.- Hubble M3521 or equivalent on end of 6 foot cable Mating Connector - Hubble M3408.

3.3.1.2 Signal Input Cable.- See Table I.

3.3.1.3 Signal Output Cable.- See Table I.

3.3.2 Associated Accessories.-

3.3.2.1 Manuals.- Each unit shall be supplied with a maintenance manual, which lists the general description, installation, and operating procedures of the items specified herein.

3.3.3 Maximum Weight.- Each unit shall weigh no more than 800 lbs.

3.3.4 Active Devices.- All active devices shall be hermetically sealed.

3.3.5 Integrated Circuits.- All integrated circuits shall be permanently connected. Integrated circuit sockets shall not be used.

3.3.6 Replaceable Parts.- A table of spare parts by schematic reference designation shall be provided which references the schematic number. The following parts lists for the disk memory shall also be provided.

a. Component List
b. Circuit Board List
c. One Years' Recommended Spares
d. One Years' Isolated Spares

3.4 Electrical and Performance Requirements.- See system block diagram, Figure 2.

3.4.1 Data Capacity.- The disk shall hold 2.5×10^9 bits of unformatted data.

3.4.2 Organization.- The disk shall provide 4 parallel read/write heads per head address, 10 head addresses per cylinder, and 411 cylinders per unit.

3.4.3 Data Rate.- The data rate shall be 9.677 Mbps for each of the 4 parallel channels.

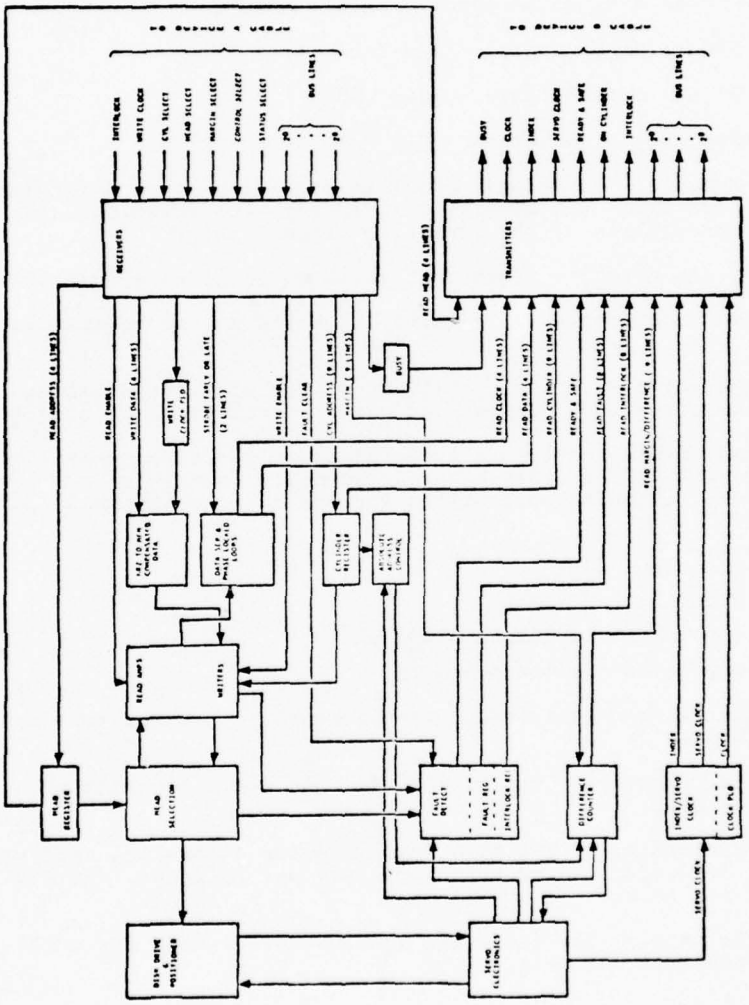


FIGURE 2. JLOCK DIAGRAM

PROCUREMENT SPECIFICATION	SPECIFICATION NO S 0 0 1 9 5	REV —
	CODE IDENT NO 94117	SHEET 4

Pin No.	Cable A (To DSU)	Cable B (From DSU)
S-Y	WRITE CLOCK	CLOCK
K-R	CYLINDER SELECT	INDEX MARK
D-J	HEAD SELECT	SERVO CLOCK
c-d	MARGIN SELECT	READY AND SAFE
N-P	CONTROL SELECT	ON CYLINDER
V-W	STATUS SELECT	BUSY
C-F	BIT 0	BIT 0
E-M	1	1
L-U	2	2
a-b	3	3
g-h	4	4
m-n	5	5
p-g	6	6
j-k	7	7
e-f	8	8
A	INTERLOCK	INTERLOCK
B	INTERLOCK	INTERLOCK
Z	GROUND	GROUND
T	GROUND	GROUND
X	GROUND	GROUND
H	NOT USED	NOT USED
I	NOT USED	NOT USED

TABLE 1 INTERFACE CABLE LINES

3.4.4 Disk Speed.- 3600±72 RPM with 208 Vac, 60 hertz after 10 minutes warmup.

3.4.5 Access Time.- 50 milliseconds average. 15 milliseconds maximum single track access. The single track access time shall be less than the disk rotation period under all of the operating conditions specified.

3.4.6 Head Skew.- The maximum skew between any two heads in a head group will be less than 1 microsecond providing no head replacement has been made. The maximum skew will be less than 5 microseconds if a head has been changed.

3.4.7 Signal Line Drives.- All signal lines shall be driven by 75110 drives as described in CDC Customer Engineering Manual BK304.

3.4.8 AC Power Requirements.- 208±10 percent three phase, 60 hertz ± 1 percent.

3.4.9 Run Current (at 223 VRMS AC Input).- Disks and carriage in motion 9.5 amps maximum.

3.4.10 Start Current (at 223 VRMS AC Input).- 50 amps/phase maximum (0-30 sec.).

3.4.11 Start Time.- The time elapsed between application of low AC (179 VAC) and generation of disk ready signal shall be ten minutes, maximum.

3.4.12 Controls and Indicators.- See Figure 3.

3.5 Environmental Service.-

3.5.1 Temperature Range.-

3.5.1.1 Operating.- 15.5°C to 32°C with a maximum gradient of 6.7°C per hour.

3.5.1.2 Nonoperating.- -34.4°C to 65.6°C with a maximum gradient of 2 per hour.

3.5.2 Humidity.- 30 percent to 80 percent relative humidity (providing there is no condensation). Operating and 5 to 95 percent nonoperating.

3.5.3 Altitude.- 1000 feet below sea level to 6000 feet above sea level.

PROP	ITEM	PREP	LINE #																				
			19	20	21	22	23	24	25	26	27	28	29	30									

START	READY	FAULT	MAINT	TEMP	0	1

Figure 3 Operator Panel

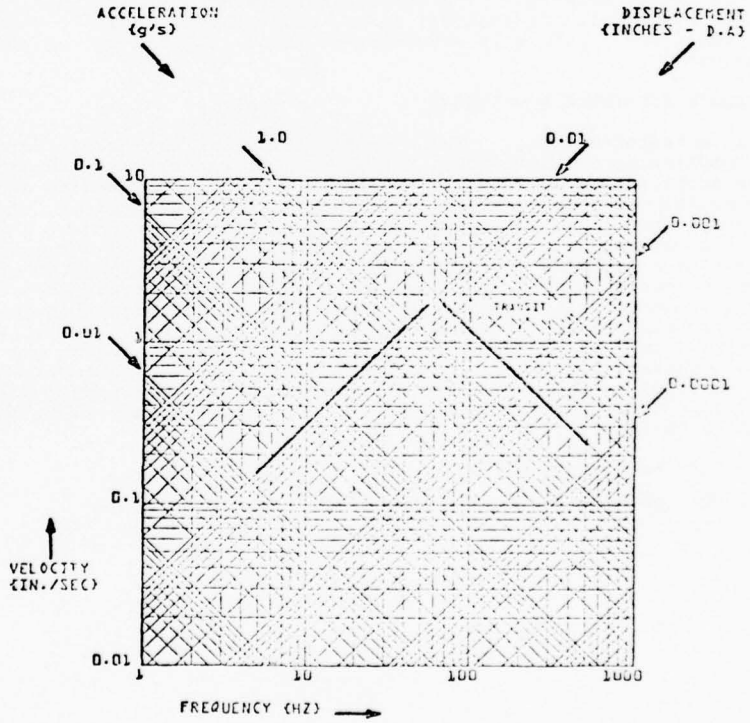


FIGURE 4 VIBRATION CURVES

PROCUREMENT SPECIFICATION	SPECIFICATION NO 8 0 0 1 9 5	REV —
	CODE IDENT NO 94117	SHEET 7

3.5.4 Shock.- Each unit shall be capable of withstanding a shock of 5 g not exceeding 10 ms in duration. The time between consecutive shocks cannot be less than 5 seconds.

3.5.5 Vibration.- Shall not be greater than shown in Figure 4.

3.5.6 Reliability and Maintainability.- Data and estimates relative to reliability and maintainability shall be provided.

3.6 Workmanship.- Each unit shall be manufactured and processed in a careful and workmanlike manner and shall be free from defects of material or construction that will affect life or serviceability.

3.7 Marking.- Each unit shall be permanently and legibly marked with the manufacturer's name or symbol and part number.

3.7.1 Panel Marking.- The visible surface adjacent to panel facilities such as controls, indicators, jacks, and sockets, shall be marked with suitable word, phrase or abbreviation indicating the use or purpose of the part.

4. QUALITY ASSURANCE PROVISIONS

4.1 Acceptance Tests.- The supplier shall be responsible for accomplishing the individual tests. Except as otherwise specified, the supplier may utilize his own facility or any commercial laboratory acceptable to Sanders Associates, Inc. Sanders Associates, Inc. reserves the right to perform any of the tests set forth in this specification where such tests are deemed necessary to assure disk memories conform to prescribed requirements. All inspection and testing shall be under the cognizance of a Sanders Associates, Inc., Quality Control Representative. The supplier shall furnish test reports showing quantitative results of all acceptance tests. Such reports shall be signed by an authorized representative of the supplier and a Sanders Associates, Inc. representative. Acceptance or approval of material during the course of manufacture shall not be construed as a guarantee of the finished product. Acceptance tests shall consist of the following:

A. Individual Tests

B. Special Tests

4.1.1 Individual Tests.- Each disk memory shipped shall be subjected to the individual tests and a copy of the data resulting from test measurements shall accompany each disk memory upon delivery. Disk memories shall bear an identification serial number such that the test results can readily be associated with the disk memory upon which measurements were observed. The individual tests shall be adequate to determine compliance with the requirements of material, workmanship, and operational adequacy. As a minimum, each disk memory accepted shall have passed the following tests:

A. Examination of Product

B. Operational Test

4.1.1.1 Examination of Product.- Each disk memory shall be examined carefully to determine that the material and workmanship requirements have been met. Physical aspects shall be in compliance with Figure 1.

4.1.1.2 Operational Test.- Each disk memory shall be operated for a sufficient period of time for the disk memory operating temperature to stabilize and to check sufficient characteristics and record adequate data to assure satisfactory operation.

4.1.2 Special Tests.- When engineering changes are made, special tests may be required for the purpose of checking the effect of any design or material change on the performance of the disk memory and to assure adequate quality control. Special tests are those tests required and agreed upon by the supplier and Sanders Associates, Inc., when it has been determined that additional mechanical or electrical design changes are necessary for improved performance/delivery/cost. Such tests may include but not preclude all the requirements of the acceptance tests.

4.1.2.1 Scope of Tests.- Special tests shall consist of any tests deemed necessary by Sanders Associates, Inc. Test procedures previously approved for the acceptance tests shall be used where applicable. When not applicable, the supplier shall prepare a test procedure and submit it to Sanders Associates, Inc., for approval prior to conducting the tests.

4.2 Test Procedure.- The procedures/data sheets to be used for conducting supplier's acceptance tests, shall be prepared by the supplier and submitted to Sanders Associates, Inc. for review and approval. Procedures shall include a list of the required support test equipment and shall detail examination method and criteria. When special tests are required, procedures shall include measurements to be made before, during and after any environmental tests. The right is reserved by Sanders Associates, Inc. to modify the test or require any additional tests deemed necessary to determine compliance with the requirements of this specification, the subcontract or purchase order.

4.3 Production Units.- Disk memories supplied under the subcontract shall in all respects including design, construction, workmanship, performance, and quality be equivalent to the first disk memory accepted. Each disk memory shall be capable of successfully passing the same tests as imposed on earlier disk memories during acceptance tests. Evidence of noncompliance with the above shall indicate a possible latent defect of disk memories already accepted by Sanders Associates, Inc., and it shall be the obligation of the supplier to make necessary corrections as approved by Sanders Associates, Inc., if such defects are proven by further tests. Disk memories which have been reworked may be resubmitted for acceptance and/or retest, with full particulars concerning action taken to correct the defects.

4.4 Rejected Units.- Disk memories which have been rejected may be reworked or have parts replaced to correct the defects, and resubmitted for acceptance. Before resubmitting, full particulars concerning previous rejection and the action taken to correct the defects found in the original shall be furnished to Sanders Associates, Inc. Disk memories rejected after retest shall not be resubmitted without the specific approval of Sanders Associates, Inc.

4.5 Changes.- No changes to the supplier's part or parts identified by this specification which effect performance, size, weight, installation or interchangeability shall be incorporated and delivered against any Sanders Associates, Inc., subcontract or purchase order unless approved by Sanders Associates, Inc.

TABLE II

SCN	Manufacturer's Part Number
	Magnetic Peripheral Inc.
800195P1	BR304

TABLE III

Source of Supply
Magnetic Peripheral Inc. 7801 Computer Ave. S. Minneopolis, Minnesota 55435 FSCM - 19333

SECTION 4

DEVELOPMENT PLAN

This section presents a plan, schedule, and cost estimate for the development of a pilot model of the standalone configuration of the Sensor Data Correlation System (SDCS). In general the plan also applies to the development of a system utilizing an existing or planned non-dedicated host. In this case the Sanders Analysis Laboratory Computer Facility, shown in Figure 4-1 would be utilized for system integration and test. The plan assumes that the initial application of the system would be for establishing, maintaining, and using a file of teletype messages similar to those contained in the NMIC 5-day file. The plan also assumes the use of the DEC RSX-11M operating system for the standalone configuration. If the major SDCS components (i.e., the DSU, Associative Processor, and Graphic 7 Display Terminal) are to be integrated into an existing or planned system using the RSX-11D or other operating system, the software written for RSX-11M would have to be transported to the other system since the Analysis Laboratory Computer Facility, as currently configured, cannot support a system as large as RSX-11D.

Although applications involving the manipulation of alphanumeric data only do not require a Graphics Display Terminal in the system, it is strongly recommended that either the SA 500 or Graphic 7 be provided as the primary operator interface for the systems. There are two reasons for this; 1) the powerful instruction set and 32 special function keys have been utilized to provide simple, single keystroke commands for interacting with the system and 2) for applications involving sensor data correlation an ability to overlay detailed maps is essential. The system as currently designed is, however, capable of operating with a GFE alphanumeric terminal, such as the Univac 1652, provided that it has a minimum of 32 user defined variable function keys and a minimum of 4K byte readily accessible refresh memory.

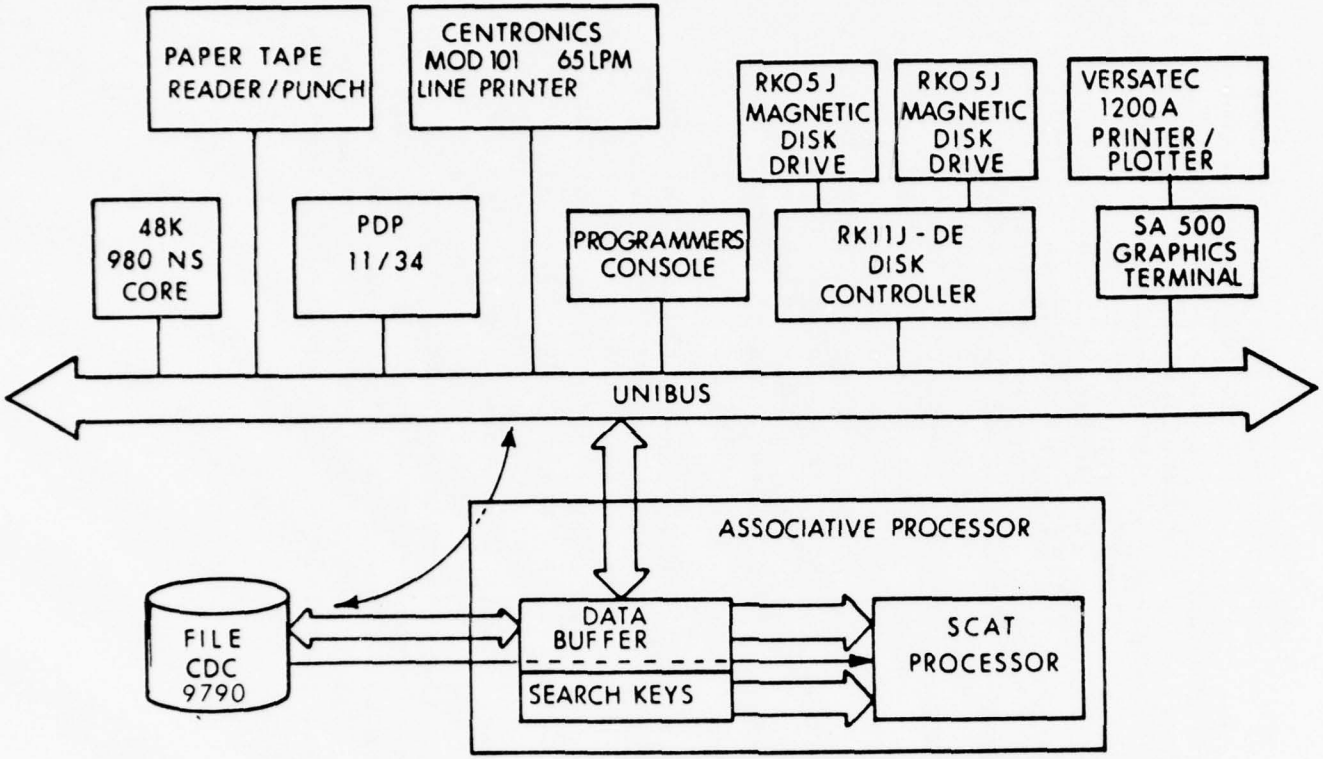


FIGURE 4-1
ANALYSIS LAB COMPUTER FACILITY (WITH SCAT FILE AND PROCESSOR ADDED)

4.1 System Fabrication, Assembly, & Debug

The schedule for development is shown in Figure 4-2. During the first 13 months of the program one Sensor Data Correlation System will be fabricated, assembled, debugged, and tested. During this period, a final Acceptance Test Procedure will be prepared and submitted for approval, an Installation Plan prepared and submitted, and a Reliability Analysis completed and reported.

The system will be designed to the standards of Best Commercial Practice and commercial temperature range components will be used throughout. All purchased material will flow through Incoming Inspection. All circuit card assemblies and subsystem modules which are fabricated and assembled at Sanders' facility will be subjected to an in-process inspection using applicable sections of Sanders Standard Quality Control Instruction Manual as a guide. The entire system will undergo formal final inspection prior to shipment to the customer's site.

The Acceptance Test Procedure will be designed to show that the specified functional capabilities of the system are being provided and that the Associative Disk File and Processor are performing correctly. The performance of the off-the-shelf equipment, including the Disk Storage Unit, the SA 500 Graphics Display System, the PDP-11 System Controller, and the PDP-11 peripherals will be demonstrated by using the standard diagnostics provided by the vendor to exercise each major component of the system.

The Reliability Analysis will be limited to two detailed MTBF calculations for single point failures of the Associative Processor and two overall system MTBF calculations for single point failures using the MTBF's for the Associative Processor and established MTBF values for all of the other, off-the-shelf, major system components. The two MTBF calculations for the Associative Processor will include one calculation for failures which result in partial system failure. A partial failure is one which because of the high degree of parallelism of the Associative Processor, results in the loss of a data and/or key channel but still permits the system to be used in a degraded mode.

4.2 Documentation

Documentation furnished during this phase will include:

- Interim Report (5 mos. ARO)

  This includes the Installation Plan and the

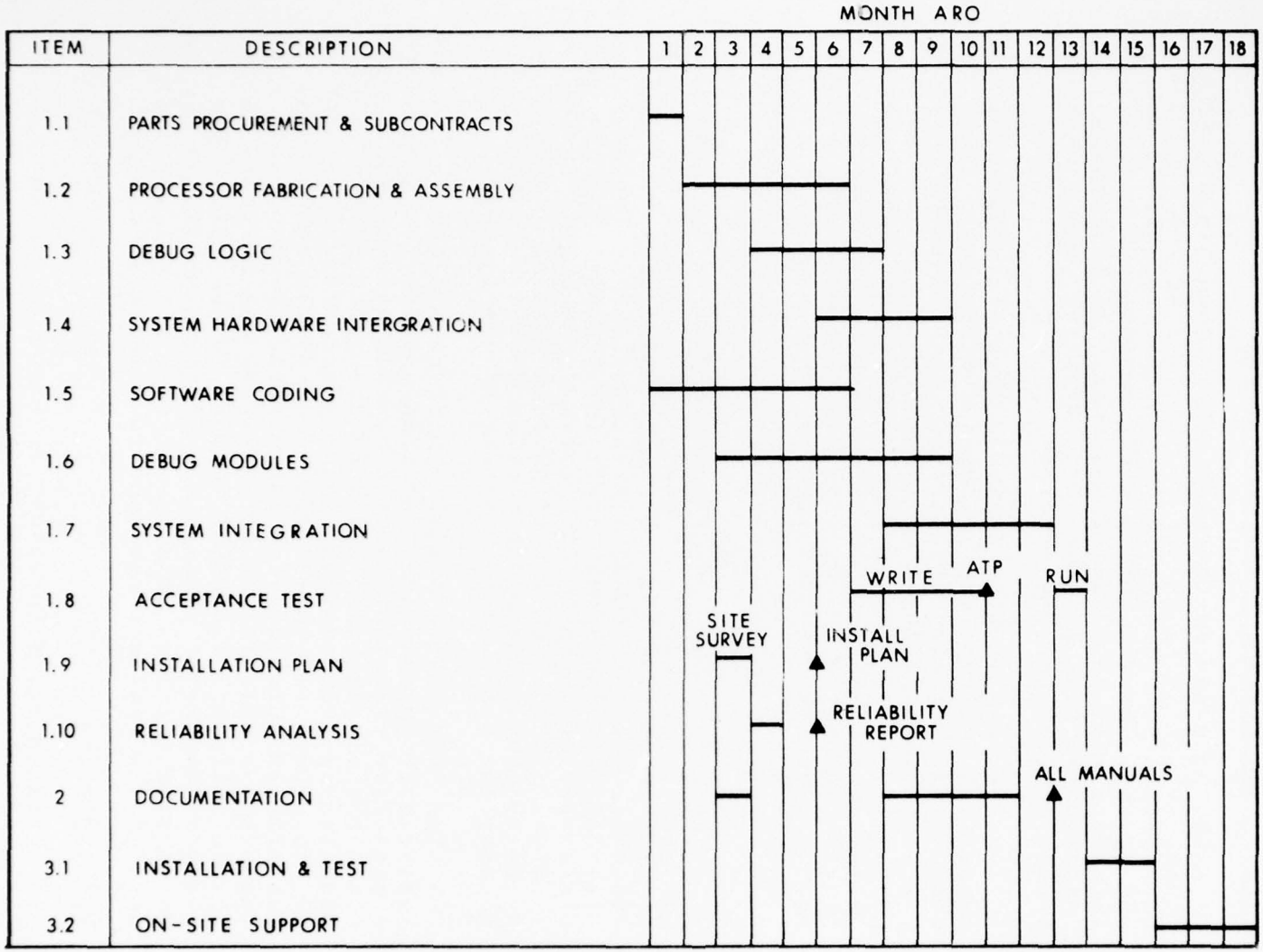


FIGURE 4 - 2 PROGRAM SCHEDULE

Reliability Report. The Installation Plan will be prepared and submitted within two months after an on-site inspection by Sanders personnel. The Plan will provide the user with specific requirements for installing the system at his facility.

The Reliability Report will present one MTBF for overall system failure and one MTBF for a partial system failure.

- Acceptance Test Plan (10 Mos. ARO)

  A preliminary Acceptance Test Plan will be prepared and submitted for approval at least two months prior to the planned date for performing the Acceptance Test at the Sanders plant. The Plan will include a detailed performance specification to which the system will be tested and a detailed, step-by-step procedure for determining whether the system meets the specification.

- System Manuals (12 Mos. ARO)

  System manuals will be available prior to performance of the Acceptance Test at the Sanders Plant. This will include a system Users Manual, a Programmers Manual, a Maintenance Manual, System Schematics, and standard manuals provided with the major off-the-shelf system components.

  The Users Manual will provide the instructional material to allow an operator to successfully interact with the system. The System Programming Manual will offer sufficient information to a programmer about the present operational and applications software to enable him to design additional applications software. The Maintenance Manual will contain a brief theory of operation as well as maintenance flow charts, timing diagrams, troubleshooting procedures, configuration details and test equipment information.

- Monthly Letter Progress Reports

4.3 Program Support

Management and Administrative

Sanders personnel will oversee the progress of the contract to insure that established milestones are being

met, that the customer is apprised of system development and that appropriate personnel are assigned to the contract as they are required. These personnel will also oversee all fiscal expenditures and obligations relating to the contract.

Expediting

Sanders will provide personnel to obtain material, keep track of long lead items, and assist in the delivery of the associative processing system after completion of the Acceptance Test.

Quality Assurance

Sanders Quality Assurance personnel will insure that all major components undergo proper incoming inspection and that the Acceptance Test Procedure is conducted along established customer guidelines. Quality Assurance personnel will also document any defects in vendor supplied components and conduct liaison with the vendor for resolution of the defects.

4.4 Long Lead Items

The proposed schedule assumes timely delivery of the following deliverable long lead items:

PDP-11/45 and peripherals (6 months ARO)
CDC 9790 Disk Storage Unit (3.5 months ARO)
SA 500 Graphics Display Terminals (4 months ARO)

Since the stated delivery for the PDP-11/45 equipment is 10 months ARO and the stated delivery for the CDC Disk is 8 months ARO, orders for these items must be placed in May 1977 if this schedule is to be met, assuming a 1 September 1977 start date.

4.5 On-Site Support (Optional)

Sanders can provide engineering services to assist and instruct the User in the operation of the system and to develop any additional applications software which operation of the system in the User environment may indicate to be desirable.

In addition, Sanders will provide such on-call maintenance service as required to maintain the system to the level of performance demonstrated during the Acceptance Test. Maintenance of Digital Equipment Corporations' equipment and Control Data's equipment by qualified and cleared personnel is to be negotiated.

4.6 Cost Estimate (Fabrication and Test Phase)

The estimated cost for fabricating and testing one prototype Sensor Data Correlation System is about $930,000 This cost covers all hardware items, software packages, engineering and programming time, and documentation required to provide a fully operating system at a designated User site. The estimate assumes:

133% Engineering Overhead
116% Manufacturing Overhead
10.8% Materials Handling
19.8% G&A
15% Fee

Cost itemization for the prototype system is given in Table 4-1 with item cost rounded to the nearest $1,000.

The estimate includes about $200K cost for hardware including $18K materials for the A/P Processor. It also includes about 25 man months of engineering, 43 man months of programming, 17 man months of technician, and about 25 man months of program management, administration, and quality assurance. Rates used for the estimate are those in effect in August 1977.

Optional Capability

A recommended option is to expand the data base utilities software module to support additional analyst's working files. With this option each analyst would have his own individual area to store messages of long term interest. If exercised within 60 days ARO, this option would cost an additional $28K; if exercised after 60 days ARO at Sanders, it would cost an additional $39K; and if exercised after system delivery, it would cost an additional $47K.

TABLE 4-1

SDCS COST BREAKDOWN

QTY	ITEM	REF.	TOTAL COST
1	CDC 9790 DSU, interconnecting cables, maintenance, and manuals	Table 3-1	$ 44K
1	PDP-11/45 and all peripherals, maintenance, and manuals	Table 3-2	112K
1	SA 500 Graphics Display System with GSS-3 software, maintenance and manuals	Table 3-3	33K
1	A/P Processor wired and assembled	Table 3-4	66K
1	A/P Processor Debug		95K
1	Software Development, Debug, and recode		175K
1	System integration and checkout all interconnecting cables, all system manuals		140K
1	Prepare and Perform ATP		40K
1	Installation & checkout at User Site		50K
	Engineering management, administration, expediting and QA		155K
1	Reliability Analysis		6K
1	Travel & Subsistence		14K
			$930K

SECTION 5

This section contains a preliminary system functional specification to which the system could be tested and a preliminary test plan for acceptance testing. The plan indicates the approach to testing the system and does not describe specific test method or test procedures. These would be fully developed in detail during the fabrication phase.

5.1 System Functional Specification

5.1.1 Overview

The Sensor Data Correlation System (SDCS) is a data storage and retrieval system which is capable of retrieving desired records on the basis of content. The basic unit of information stored within the SDCS is a message averaging 175 words in length. A minimum storage capacity of 18,000 such messages is provided, and an expansion storage option of up to 650,000 messages is available. The system reads each message in the data base correlating the presence, absence, proximity, and logical relationships between words or groups of words in the message text and an operator defined algorithm of keywords. When a match occurs, either all or part of the message may be retrieved as specified by the analyst. Other analyst specified responses provided with the system are discussed later in this specification.

Originally, the system was conceived as a device to accumulate and correlate messages from a variety of sensors then generate target profiles. It was clear however that such a system would have application in any automatic data processing (ADP) application where no clear guidelines exist for filing and retrieving data or where those guidelines are frequently changing. All of the information stored in such a content addressable archive is available for retrieval. This is in marked contrast to the commonly used indexed systems where messages are tossed into topic bins based on subjects of interest at the time of filing. The rest of the message information in indexed systems is unretrievable i.e., lost.

The prototype SDCS will be delivered as a standalone system which is batch loaded by magnetic disk. With suitable interfacing the SDCS can be used as an on-line adjunct to a user information processing system.

5.1.2 Principle System Components

The SDCS will consist of the following principle components or equivalents:

CPU	Digital Equipment PDP 11/45-FS
CPU Memory	64K 980 nanosecond core
Paper Tape Reader/Punch	Digital Equipment KW 11P

Line Printer & Controller	Digital Equipment LA 11
Disk Transport & Controller	Digital Equipment RK11J-DE
Disk Transport	Digital Equipment RK05J-AA
Graphics Terminal	Sanders Associates SA 500
Associative Processor	Sanders Associates SCAT-16
Disk Storage Unit	Control Data CDC 9790

All of the above components will be interconnected by the Digital Equipment UNIBUS with the exception of the CDC 9790 Disk Storage Unit which as a dedicated cable linking it to the Associative Processor. The UNIBUS is a component within the PDP 11/45 CPU. Figure 3-1 shows the electrical interconnections between the principle components.

5.1.3 System Capabilities

5.1.3.1 Operator Interface

The primary operator interface with the system will be the SA 500 graphics terminal. The alternate control point for diagnostic tests of the SDCS will be the programmers console provided with the PDP 11/45 CPU.

5.1.3.2 System Disks

The SDCS will have two magnetic disk drives which will be used to store the RSX-11-M operating system, input message data to the system, and provide scratch area to format and deformat messages. Capacity of each disk shall not be less than 1.2 million bytes.

5.1.3.3 Application Program Load & Edit

Application programs may be loaded into the SDCS by paper tape or disk and may be copied to paper tape, disk or line printer. The programmers console may be employed to create or edit applications programs.

5.1.3.4 Main Data Base

The main data base will reside on the CDC 9790 disk storage unit. The main data base will be updated by taking source messages from one of the RK05 magnetic disk units, formatting the messages for associative

search, and writing the formatted version to the CDC 9790 disk storage unit via the associative processor.

5.1.3.5 Search Control

The operator at the graphics terminal will be able to compose search algorithms and specify the information that he wishes to extract from messages that satisfy the algorithm. Up to thirty two text words may be used in the algorithm and those may be related to each other by the logical operators AND, OR, EXOR, NOT, NAND, NOR AND EXNOR. Additionally, eight of the textwords may also have order and proximity specified. When brevity codes are used in messages contained in the data base, brevity coded elements may be substituted for textwords in the algorithm.

5.1.3.6 Information Retrieval

The operator may specify the following information to be retrieved when a message in the data base matches the algorithm:

- Entire Message
- Location of the message within the data base
- Message Header
- Indication of which elements within the algorithm were satisfied.
- Number of messages satisfying the algorithm

5.1.3.7 Disposition of Retrieved Information

The operator may specify how the retrieved information is to be handled:

- Display on the graphic terminal
- Print out on line printer
- File on RK05 magnetic disc

5.1.4 Configuration and Performance Specification

Table 5-1 summarizes the system configuration and performance requirements as specified in the referenced paragraph of the Statement of Work PR I-6-4604. In general, the acceptance test will be designed to demonstrate conformance with the applicable performance specifications listed. It is not intended, however, that the configuration requirements (e.g., capacity of the disk file or the orthogonal memory) will be directly demonstrated by the test but will be proven either indirectly or by applicable system documentation.

TABLE 5-1

SYSTEM SPECIFIED CONFIGURATION & PERFORMANCE

SOW Ref. Paragraph	Characteristic	Spec. Value
4.1.1	File Capacity	50 Mbytes min.
4.1.1	Expanded File Capacity	200 Mbytes min.
4.1.1	File Transfer Rate	4.0 Mbytes/sec. min.
4.1.2	Processor compare capability	equality or inequality
4.1.2	Processor speed	matched to transfer rate of file
4.1.2	Fractional search capability	8 bytes of comparand with 100% of file record data or 16 bytes of comparand with 50% of file record data or 24 bytes of comparand with 33.3% of file record data
4.1.3	High speed program storage	1024 bytes of key min.
4.1.4	Algorithm Links	AND, OR, WITH
4.1.4	Terms/algorithm	Up to 24
4.1.5	Orthogonal Memory capacity	12,000 data bytes min.
4.1.6	System Controller	PDP-11/45 or equivalent
4.1.7	System Interaction I/O	Graphics Terminal
4.1.7	Display Refresh Memory	4X2048 character pages min.

TABLE 5-1 CONT.

SOW Ref. Paragraph	Characteristic	Spec. Value
4.3	Message Retrieval Time	9 sec. max. using up to 20 keywords linked by AND, OR, NOT
4.3	Disk File Capacity	18,000 messages with average of 175 words/message plus 32 bytes of header data
4.3	Operator Interactive Support	Graphics Terminal for keyword entry & retrieved message display

Two comments relative to the specifications in Table 5-1 should be made:

1) The theoretical average disk transfer rate under nominal conditions is 4.02 Mbytes/second. This assumes nominal AC line conditions for the DSU and that the track-to-track seek time is always less than the disk rotation time. The latter requirement will be incorporated into the Sanders DSU purchase specification even though the individual parameters (15 ms max, and 16.67 ms nominal, respectively) in the CDC equipment specification implies that this will always be the case. However, since disk transfer rate varies with AC line conditions, the specification for this parameter should be changed to read:

   "4.1.1 Associative disk file with a minimum capacity of 50 million 8-bit bytes expandable to 200 million bytes and having a minimum average data transfer rate of 4.0 million bytes under nominal operating conditions."

2) The system message transfer rate is highly dependent on the statistics of the data base including standard deviation as well as mean message length, average number of tuckwords, and frequency of occurance of punctuation and control characters. Although it is expected that the 9 second maximum retrieval time requirement will be met, it cannot be guaranteed without a detailed specification of data base structure. Therefore, the specification for this parameter should be changed to read:

   "As a goal, the system shall be capable of retrieving a message with up to 32 header search keys and/or text keywords in 9 seconds or less."

5.2 Preliminary Test Plan

The preliminary test plan for the SCAT SDCS is intended 1) to exercise the major modules of the system independently to the confidence level, 2) to functionally exercise the associative processor and 3) to demonstrate the major software modules provided with the system.

5.2.1 Module Tests

Listed below are the major modules of the SCAT 16 System and their corresponding tests:

MODULE:	TEST:
PDP 11/45 Processor	Standard DEC Diagnostic (X/11 Exerciser)
64K Memory	Standard DEC Diagnostic
RK11D Disk Controller and Dual RK05 Drive	Standard DEC Diagnostic
PC11 Paper Tape Reader/Punch	Standard DEC Diagnostic
LA 11 Line Printer	Standard DEC Diagnostic
Decwriter	Standard DEC Diagnostic
SA 500 Graphic Terminal	Standard Sanders Diagnostic
Orthogonal Memory	OM Diagnostic
DCU and Disk	DCU Diagnostic
AU/CIU	AU/CIU Diagnostic

The off-the-shelf equipment included in the system is tested using standard diagnostics provided by the vendor. Three diagnostics to exercise submodules of the associative processor are also supplied. These diagnostics are not exhaustive but do test the functions these devices must perform for the system to operate correctly.

The OM diagnostic tests the orthogonal memory as a standard memory. Various bit patterns are written into the OM buffer and then verified. The result of this test is a Go/No go indication of proper memory performance.

The DCU Diagnostic (short form) tests the CDC 9790 disk and controller. Included in this diagnostic are checks for seek times, read/write capability and hard errors such as CRC. The result of this test is a go/no go indication of properly functioning disk. The long form of the DCU diagnostic may be run upon request but execution time is over 2 hours. This form includes verifying read/write capability over the entire disk and a more

complete check of seek and access times. Note the search related functions of the DCU are not tested by this diagnostic.

The AU/CIU diagnostic exercises the complete capabilities of the AU/CIU modules. A series of prepared test data patterns, key patterns, algorithms and search modes are used in this diagnostic. The patterns are designed to check all functions of the AU/CIU. After each search is executed all intermediate and final results within the AU/CIU modules are verified.

5.2.2 Associative Processor Functional Tests

The Associative Processor performs two major functions. First, it acts as a 300 MBYTE disk for storage and retrieval of files. Secondly, it has the capability to search the disk associatively between limits and present the results to the host processor in a variety of forms.

The ability to read and write the AP disk was shown during the DCU diagnostic and will be further demonstrated in the system functional test. The Associative Processor functional tests center around demonstrating the Associative Processor's search capability.

5.2.2.1 Approach

Even a simple exhaustive test of the Associative Processor run against a fixed data base would take many days to run. Instead the approach to testing the Associative Processor is to demonstrate the proper functioning of various submodules of the Associative Processor under "Worst Case" conditions. These submodules are tested by running prepared search algorithms that exercise the particular submodule. Thus the submodules are tested individually but in concert with the other submodules of the Associative Processor. It is important to note that these tests do not divorce the submodule from the Associative Processor and test the submodule independently; rather a search algorithm is run normally and the results are screened to insure that the submodule performed its function accurately.

Since the performance of the system is data base dependent, three data bases are used to test the system. Prepared searches are run against the different data bases to test various facets of the Associative Processor search. The result of each search will be displayed in standard format. The left side of the SA 500 will

contain a list of all hits (message ID numbers and other data). The right side is used to display the text of messages. The bottom left corner displays the number of hits and the elapsed search time.

5.2.2.2 Data Bases

The first data base contains 48 messages. All messages contain the same 48 non-tuck words. The next message is identical to the previous with all the words rotated 1 position and the last word wrapped around to the first. This data base is called the rotated data base (RDB). This data base is useful in testing the multi-channel functions of the Associative Processor because each message in the data base is the same except that the actual words appear on different channels in the Associative Processor.

The second data base is a collection of news briefs. These messages are similar in characteristic to those expected in the operational system. This data base is called the typical data base (TDB) and is useful in demonstrating functions of the Associative Processor against a "normal" data base.

The final data base contains messages that consist of words containing all W's. This is the worst case data base (WCDB) because the Associative Processor cannot skip byte slices and thus timing tests can be made under one worst case condition.

5.2.2.3 Searches

A set of prepared searches are used by the Associative Processor functional tests. These canned searches are created using the standard entry, edit and compilation modules and the objects are stored as RK-05 Disk Files. Searches are executed by typing the search command on the SA 500 display and specifying the appropriate canned search to execute. Editing the Data Base is performed using the standard modules included in the system.

5.2.2.4 Submodule Tests

The major submodules of the Associative Processor are the Disk Control Unit (DCU), the Computer Interface Unit (CIU) and the Analysis Unit (AU).

DCU Tests

The read/write capability of the DCU was demonstrated

by the DCU diagnostic. No special individual test of the DCU's search mode is supplied rather the successful completion of all submodule tests will demonstrate that the DCU functioned correctly in the search mode.

CIU Tests

Many capabilities of the CIU were demonstrated by the memory and AU/CIU diagnostics. Most of the other capabilities of the CIU are demonstrated by the successful completion of all submodule tests. There will be at least 1 CIU test to demonstrate the various search modes supported by the CIU. They are start/stop, transfer continuous, and count hits.

AU Tests

The major submodules of the AU are the processing modules, the link analyzer and the analysis controller.

- Processing Submodule Tests

  The processing module contains the memory module and comparator register file. The memory module contains both the data and keys and has already been tested. The comparator file does the Byte-by-Byte comparison of keys and data to determine key matches. The comparisons supported by the comparator register file include: =,>,<, don't care and their inverses. This submodule is tested by designing a set of search algorithms that fully exercise all the comparator register files functions. These search algorithms are run against the rotated data base to insure that all 16 channels and their associated comparator register files are functioning correctly.

- Link Analyzer Submodule Tests

  The major functions of the Link Analyzer are Quote Analysis and Link Analysis. The Quote Analyzer keep a running 8 non-tuck word history of key strikes and performs order and proximity analysis of key strikes. The Quote Analyzer is capable of determining the order of keystrikes and the proximity of keystrikes within the range of 2 to 8 non tuckwords. This submodule is tested by designing a set of search algorithms that fully exercise the capabilities of the Quote Analyzer. The Link Analyzer keeps a single history of key strikes over an entire message and determines if the results of the quote

and algorithm history should result in a hit. Links supported by the Link Analyzer are AND, OR, XOR, QUOTES, NOT EQUAL, (, and). The Link Analyzer is tested by designing a set of search algorithms that include the complete set of links. In the typical data base are known hits and near-hits to the prepared searches. The searches are run and the results are verified that all hits are found and no non-hits are found.

- Analysis Controller Submodule Tests

  The Analysis Controller insures proper transfer of data, keys, and status across the various analysis unit buses. No specific test of the Analysis Controller functions is supplied. Rather, the successful completion of all submodule tests will demonstrate that the Analysis Controller is functioning properly.

5.2.2.5 Associative Processor Functional Test Conclusion

Functional testing of the submodules of the Associative Processor demonstrates the Associative Processor's capability to read, write, search a data base, and associatively retrieve information from a data base.

5.2.3 SDCS Functional Tests

The major functions provided by the system are:

1. Message Entry, Retrieval and Edit
2. Algorithm Entry, Compilation, and Edit
3. Search Execution

Each of these functions are demonstrated by the system functional tests. Detailed descriptions of the following operations will be available after the software is completely flowcharted. Provided at this time is a general outline indicating the sequence of operations.

5.2.3.1 Messages

Enter a new message using the message editor. Store the message and retrieve by message accession number. Update the retrieved message using the message editor and write the file back out. Retrieve and verify updated version.

5.2.3.2 Algorithms

Create a new algorithm to search for the new

message using the algorithm editor. Compile algorithm and store result in an RK-05 Disk File. Recall stored algorithm and update source. Recompile and store updated version into same RK-05 Disk File.

5.2.3.3 Searching

Execute search using the algorithm created above. Verify expected results. Re-execute algorithm specifying other output options and verify results. Experiment with updating messages and algorithms to obtain different search results.

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APPENDIX A

SCAT APPLICATIONS SOFTWARE FUNCTIONAL SPECIFICATION

A.1 INTRODUCTION

The SCAT software will provide software modules which are capable of performing the functions listed in this document when working in conjunction with the SCAT hardware system as it is currently envisioned.

The hardware system consists of a PDP-11/45 processor with a Decwriter terminal, 128K bytes of memory, two RK-05 disks, and paper tape reader and punch. Connected to that will be the associative processor with a 16K byte memory and a 300M byte associative disk file (ADF). The primary user terminal for SCAT will be a Sanders 500 graphic display and keyboard.

A.2 RESTRICTIONS, REFERENCES, AND ASSUMPTIONS

The software will be based entirely on information contained in this document. No data from prior specifications or other documents shall be included except by specific reference.

A.3 OPERATING SYSTEM

The SCAT software will operate as several tasks designed to run under the RSX-11M operating system provided by DEC. The major tasks listed below will not execute concurrently. Each must be initiated from the PDP-11 control terminal (Decwriter). Some software revision will be required if more than one user terminal is to be on line at a time.

The major tasks to be provided are:

1. ADF directory and file initialization.
2. Batch input records from an RK-05 disk pack to the ADF active file area.
3. Operate the Sanders 500 graphic display as a single on-line SCAT terminal.

Optional tasks which have been considered in the design but not fully designed at this time are:

4. Allow user to modify ADF directory allocations and move ADF data accordingly.
5. Recover an ADF directory from the file name data on the ADF.

A.4 ASSOCIATIVE DISK FILE (ADF)

The Associative Data File (ADF) has a capacity of almost 300 megabytes (297,861,120 bytes) in 24,240 sectors of 12,288 bytes each. When the file is initialized, each file is assigned a name and a fixed cylinder location. The system will have an active file area for daily input and a permanent storage area for messages which the operator decides to retain. The size and name of each file will be defined by the user before initialization time of the ADF.

A.4.1 Formats

A.4.1.1 Active File Area

This area will be defined large enough to accommodate at least five days input messages under most circumstances. If message traffic is higher than expected, or if longer retention times are desired, the area assigned to this area can be increased. When input is slow, messages will remain in the active file area more than five days.

The active file area will be cyclical in nature. When the physical end of the area is reached then the next message will be written in the first sector of the area. The oldest messages stored will be overwritten. The active file area will be divided by the system into several "day files". The system will create a file with a name representing the date that messages are input, for example "OCT23". Addresses in the directory which define the beginnning and end of each day file will be updated as records are input.

A directory will be maintained which will reflect the status of the ADF. This will be stored on the system disk and will be updated when necessary. The directory will contain the name and the beginning, last used, and ending addresses for each file in both the active and permanent file areas.

The initial system will allocate 6,000 sectors for the five day active file area. This can be adjusted to reflect changes in the actual rate of input.

As each input file is completed, the end address will be set a few sectors ahead of the actual end of data to allow space for appending new or edited messages.

After 5 or more days, depending on the actual quantity of data received each day, the total active file area will become full. This will cause a wrap around to the beginning of the active file area and the file for day 1 will have some or all of its sectors overwritten.

A.4.1.2 Permanent File Area

In addition to the active file, there will be an area for permanent storage. It may be divided into several files by the user to provide for storage of records (messages and/or commentary) which the analyst operators desire to retain. The file areas will be assigned names and allocated a certain area of the ADF. Messages of interest which are found in the active file may be edited by the operators and filed in one or more of the permanent areas.

These files may be organized by geographic areas, individual operators, subject codes, or any other criteria desired by the operators. In the initial system, messages in the permanent file areas will not be deleted except by specific operation action. Optionally, a routine could be added later to periodically purge messages of more than a certain age, such as 90, 180 or 360 days.

A.4.2 ADF Directory Format

The directory contains the beginning and ending sector address for each file, the filename, and the next sector and byte address within the sector at which to append a new or edited message.

The directory will also contain information regarding the total active file (within which there will be many day files) such as the beginning and ending address, start address for the next day file and a pointer to the next location within the directory to store information for a new day file.

A.4.3 ADF Initialization

ADF initialization will be run as a part of system generation. The ADF Directory will be created and initialized. Each sector of the ADF disk will be initialized to contain a dummy message with a format byte which will identify the message as a sector header so that sector header messages will not be searched by normal message

search procedures. The sector header message will contain one byte slice. The following information will be present:

1. Sector header message format byte
2. Location of this sector (sector address, location zero)
3. Location of next message. (first data message in sector)
4. First location in sector available for new data.
5. Name of the file of which this sector is a part.

A.5 RECORD FILE INPUT

The primary source of input shall be files loaded onto RK-05 disk packs by external systems. Records to be entered will be written on one or more files which are compatible with the RSX-11M operating system and the requirements defined below.

The input process for each file shall consist of:

1. Reading an input message.
2. Assigning a unique accession number to each message.
3. Formatting and checking the header.
4. Blocking the text.
5. Packing blocked messages into 12K byte pages
6. Writing the packed sectors to the ADF.
7. Repeat until all messages in input file processed.

A.5.1 Batch Input Processing

Records to be entered shall be stored on the RK-05 as a file of variable length records. Each logical record as retrieved by the standard disk I/O routines within RSX-11M shall contain only one message. All the records within one file shall be the same format.

A.5.1.1 Task Initiation

The operator will initiate the batch input task and provide it with the name of a file containing input records and the format of those records. This task will automatically enter the input into the active file area in a file named with the current data, e.g., "OCT23". If a file with that name exists, the input will be appended to that file. If no file so named exists, one will be created following the most recent previous date.

If additional input files of the same or different format are to be processed, a new input file name and format may be entered after the first file has been processed.

A.5.1.2 Record Input

The input task will read each record in the input file, encode the header data, block the text data, and write the records to the ADF. Additionally, each record will be assigned an Accession Number as it is entered into the SCAT system.

A.5.1.3 Accession Number

Each message input or created will be assigned an accession number. Accession numbers will consist of eight octal digits. When a record is edited and/or copied, the operator will have a choice of retaining the old number or assigning a new number. This will provide for 16,777,216 messages to be acquired before the number sequence will repeat.

A.5.2 Message Header Format

As initially delivered, the SCAT system will provide for batch input of only one record format, that of teletype messages per ACP-127E. An additional format for search algorithms will be provided without any batch input capability. These format definition tables will be provided with the system. The user may add other format tables to the system after delivery.

Each format table must contain:

1. The format name
2. Graphic data length, (upper limit, may be zero)
3. Textual data length, (upper limit, may be zero)
4. Header data length, (fixed number, may be zero)
5. List of all single valued header attribute names and their position in the header.
6. List of all multi-valued header attribute names and their positions in the header.
7. List of coded values or numeric range and conversion algorithm for each attribute.

Additional data to describe the input format and how the header data is encoded and put into the blocked header must be provided if other format batch inputs are to be accepted.

A.5.3 Blocking Process

The message header information will be encoded and blocked according to data contained in the input description of the format definition table. Text blocking will consist of byte translation into characters or punctuation; separation of words; tuckword recognition, and encoding; and blocking the remaining textwords, tuckwords, and punctuation into a format which allows fast searching of the text. The initial system will not attempt to count the sentences or paragraphs within a message.

A.5.3.1 Text Byte Translation

When input, all text bytes will be either carriage return, line feed, tab, or a printable code in the range of 240 octal to 337 octal. Tab codes will be expanded into the indicated number of spaces (move to next higher column which is a multiple of 8) and then each byte will be examined and punctuation codes will be translated. This will divide the text into words (strings or characters) separated by one or more punctuation symbols. Codes used in addition to characters and punctuation include:

NULL - used to fill out each row of text block except the longest.

REPEATED SYMBOL - first of three bytes used to compress strings of identical bytes.

BROKEN WORD - prefixes parts of words in excess of 32 characters.

1. The following 6 symbols and 2 sequences will be translated according to the context in which they appear: (ASCII octal code in paren.):

- Single quote or apostrophe (247)
  This will be a character if it is both preceeded and followed by a letter. Otherwise it will be a punctuation symbol.
- Comma (254)
- Decimal - period (256)

- Colon (272)
  These will be punctuation except if they appear between two numeric digits in which case they will be characters and the string containing them will be treated as one word.

- dash - minus - hyphen (255)
  This will be a character if between numeric digits or letters. If between character and carriage return, both will be deleted. Otherwise it will be punctuation.

- Slash (257)
  This will be a character if between numeric digits, and punctuation.

- Repeated Characters
  Any string of four or more of the same character will be treated as a punctuation symbol and will be encoded into three bytes:

  1. byte repeat code
  2. the byte which is to be repeated.
  3. a count (4-72) of the number of identical bytes.

- Carriage Return and Line Feed (212 & 215)
  When either CR of LF or any consecutive sequence of them is found, they will be translated into a number of new line bytes equal to the number of line feeds in the sequence, but not less then one if only carriage returns are in the sequence.

2. The following 42 bytes will always be characters:

number or pound sign	243
dollar sign	244
per cent	245
ampersand	246
plus	253
digits 0 thru 9	260-271
at sign	300
letters A thru Z	301-332

3. The following 16 bytes will always be punctuation:

space	240
exclamation point	241
double quote	242
parentheses	250-251
asterisk	252
semicolon	273
greater than	274

equal to	275
less than	276
question mark	277
brackets	333-335
back slash	334
up arrow (or caret)	336
back arrow (or under-score)	337

The 256 possible data bytes are divided into five categories so that numeric comparisons on a byte can determine if a byte is a part of a word or not. The initial byte assignments are given below. Other codes within each category may be assigned. The reserved category could be used either to include lower case letters and additional sysmbols, or to implement the long word compression scheme described in 5.3.3.

CATEGORY	CODES	TOTAL	DEFINED	SPARE
Special	000-007	8	3	5
Punctuation	010-057	40	23	17
tuck words	060-237	112	50	62
characters	240-237	64	47	17
reserved	340-377	32	0	32

A.5.3.2 Tuck word Recognition and Encoding

Tuck words are those words which occur so frequently in the text being searched that they will be useless as text search keywords, such as "and", "the", "from". The SCAT system will reduce each such word in the input text to a single byte tuckword code for storage on the ADF. When a message is retrieved, the tuckword bytes will be translated back to the original word. In searching the text, a tuckword may be used in a phrase as long as it is not the first word. For example, "surface to air" could be searched for but "from the missile" could not.

The preliminary list of tuckwords will be taken from Table A-1 lists 80 tuckword candidates with frequency data taken from Kucera and Francis and from DDC 10 million word data base.

A.5.3.3 Optional punctuation and long word compression

Other compression techniques can be used to increase the packing density of the blocked data by reducing the number of nulls stored. The advantages of increased density are faster search times and more storage capacity. The disadvantages are more time spent in

TABLE A-1

80 TUCK WORDS

Tuck Word	No. Char/Freq (%) 1	2	3	4	5	DDC Rank	Tuck Word	No. Char/Freq (%) 1	2	3	4	5	DDC Rank
THE			7.2			3	WE		.12				
OF		3.2				2	HIM			.10			
AND			2.5			1	BEEN				.24		12
TO		2.4				4	HAS			.34			18
A	2.4					7	WHEN				.19		
IN		2.3				5	WHO			.30			
THAT				.93		22	WILL				.44		8
IS		.83				11	MORE				.21		32
WAS			.81			26	NO		.14				
HE		.72					IF		.12				
FOR			1.09			6	OUT			.18			
IT		.54				34	SO		.09				
WITH				.64		13	SAID				.46		
AS		.58				15	WHAT				.11		
HIS			.48				UP		.19				
ON		.78				10	ITS			.20			40
BE		.59				9	ABOUT					.17	
AT		.72				21	INTO				.13		33
BY		.57				17	THAN				.16		
I	.21						THEM				.11		
THIS				.36		14	CAN			.11			35
HAD			.32				ONLY				.12		
NOT			.29			37	OTHER					.18	
ARE			.37			16	NEW			.27			
BUT			.32				SOME				.13		
FROM				.40		23	TIME				.12		
OR		.20				24	COULD					.10	
HAVE			.30			20	THESE					.08	
AN		.35				19	TWO			.20			
THEY				.30			MAY			.10			44
WHICH					.28		THEN				.08		
ONE			.24				DO		.07				
ALSO				.14		36	FIRST				.18		
WERE				.28		28	ANY			.11			
HER			.14				NOW			.10			
ALL			.20			29	SUCH				.08		27
SHE			.09				OVER			.13			
THERE					.21		MOST				.10		41
WOULD					.28		MADE				.12		31
THEIR					.26		AFTER					.17	
						% TOTALS:		2.61	14.51	16.49	6.03	1.73	
						TOTAL FOR ALL WORD LENGTHS:							41.37%

blocking the data and a slight increase in the time to unblock data. Also compression within a word may interfere with matching keywords containing wildcard characters.

A.5.3.3.1 Punctuation Sequences

Optionally, common punctuation sequences could be contained in a table similar to the tuckword table. In some cases the sequences could replace the single punctuation symbol. Likely candidates for the punctuation table are:

period space
comma space
exclamation space
space double quote
double quote space
space single quote
single quote space
space left parenthesis
right parenthesis space

A.5.3.3.2 Character Sequences within Words

An additional possibility is that letter sequences within words could be encoded. This will not be provided in the initial system. If implemented, this would have the effect of shortening the words in which these occur. If one or more sequences occur in the longest word of a text block, the block will be shortened and the packing density of the data on the ADF will be increased. Such sequences might include:

5- ATION

4- IGHT SION ANCE ENCE ABLE NESS

3- ING SUB CON ATE OUS

2- TH PH QU CH LY

Obviously the longer sequences will result in more efficient packing of the data, but also they are less likely to occur. A study of the frequency of the sequences in the data actually used and the length of the words in which they appear (actually word and following tuckwords) could be made to determine which sequences, if any, should be used. Also tradeoffs such as including both ANCE and ENCE or just the three byte sequence NCE should be studied.

A.5.3.3.3 Maximum Block Length

The maximum block length for text has been set at 32 bytes. Provision has been made for those lines in which the word and its following punctuation and tuckwords exceed the specified limit.

The compiler will detect keywords greater than the block length and give a correct search algorithm for the first part, but the continuation may not be used as a search key.

A.5.3.4 Text Word

A word of text shall be defined as a string of one or more contiguous characters after the tuckwords and punctuation have been identified. Characters may be alphabetic, numeric, or special symbols. Any punctuation or tuckword will terminate a word. Any "word" of more than 32 characters will be divided into pieces. Only the first piece of a word so broken may be used as a search key.

A.5.3.5 Blocking Format

Each message will have a format slice containing pointers to the header of this message, the text of this message, and the format slice of the next message. Graphic data if any will be between the end of the header and the start of the text.

Blocking of text will be done by setting up an array of 16 x 32 bytes of memory. Each array will be preceeded by a format byte slice of 16 x 1 bytes. After the array has been filled, the location of the next available position following the longest textword and the tuckwords and or punctuation following it will be put into the format byte slice. The first character of each of the first sixteen words and the second character of each into the second column of each row. Any coded punctuation or tuckword bytes between words will follow the last character of each word. Nulls (octal 000) shall follow punctuation or tuckword bytes. After all sixteen words and their following bytes have been transferred, the longest row in the block will be determined and put into the block format slice.

The process will be repeated for groups of 16 text words until all the textwords of the message have been blocked at which time the message format slice pointer to the next message will be provided.

A.5.4 ADF Format

Each record on the ADF must have one format byte slice of 16 bytes. This will define the format of the record. Each format must be defined in a format definition table which will describe the attributes, text, or graphic data areas of the record. In addition, the format definition table will list the codes for all attribute values. Header information must be fixed length. Text or graphic data may be variable length. The only format defined in the system as delivered will be that of TTY messages.

A.5.4.1 Record Format Slice

Each data record must contain the following in its format byte slice:

1. Format of this message.
2. Address of this message: track, surface, sector, location.
3. Address of next data message in this file.
4. Pointer to start of header block in this message.
5. Pointer to start of first text block in this message.

A.5.4.2 Header Data

The header of any record must be a fixed length. Each format type may have a different length and order of attributes.

For example, the header block of a TTY message will contain three byte slices containing up to eight single valued attributes followed by two byte slices for each of four multi-valued attributes for a total of twelve byte slices.

Single valued:

1. The date the message was initiated.
2. The time and time zone that the message was initiated. (Both the time and date attributes will appear twice in the header so that two values may be compared when a range of dates and/or times is desired.)
3. A message accession number assigned when the message is entered into the SCAT system.
4. A message ID number, denoting precedence and security classification.

Multi valued:

5. Up to sixteen addressee codes.
6. Up to sixteen subject category codes.
7. Up to sixteen subject sub-category codes.
8. One message source or originator code. (Note that this is classed as a multi-valued attribute even though only one valued is permitted. This is to allow a search algorithm to specify a list of source values which will be acceptable.)

A.5.4.3 Text Data

The text area of any data record will contain one or more text blocks, each consisting of one block format slice followed by a variable number of byte slices of textwords, tuckwords, and punctuation. The block format slice will contain the pointer to the next text block in the message. The first byte of each following slice in the block will be a character of the first textword and the second character of each slice, the second textword, etc. Each block will contain 16 textwords. The block length will be the number of characters in the longest of the sixteen words plus any tuckwords or punctuation which may follow it and one additional for the block format slice.

A.5.4.4 Graphic Data

Graphic data in any format may be variable or fixed length. It will consist of display instructions for the SANDERS ADDS 500 display controller. Searches will not compare to the display instructions. If present, the graphic data area will follow the header and preceed any text area.

A.5.5 Active File Area Directory Update

Initially, an area of the ADF shall be designated in the directory as the active file area. When messages are input via the batch input task, they will be written to this area in a file with a name corresponding to the date of the system clock when the messages were entered. When the end of the designated active file area is reached, further input will be written at the beginning of the area overwriting the oldest inputs. In the initial system, no provision will be made for examining the messages which are overwritten.

Depending on the size of the active file area and the actual quantity of messages input, there may be

several daily files in this area. As new messages are input, the oldest will be overwritten in the order in which they were received. The start address of the oldest file will be updated as its contents are destroyed. If all the messages in a file are destroyed, the file name will be deleted. If new input would cause more than 12 file names to exist, the two oldest files will be combined in the directory into one file with the name "old".

A.5.6 Message Display Format Deblocking

Header deblocking will require looking up each attribute value in the format definition table and inserting the ASCII characters found there into the fixed length areas of a header display block.

Text deblocking will be performed on a byte by byte basis. Each byte will be examined and the appropriate data will be put into the output area. Character bytes will be moved directly to the output area. Punctuation bytes will be translated to the indicated symbol. Generally, punctuation bytes will include a leading or trailing space. Tuckword bytes will be translated to the encoded tuckword preceeded and followed by a space except where a non-space punctuation byte following or preceeding would create a double space. If used, the word compression bytes would be translated into a string of characters. Repeated byte groups will be expanded. Word terminators will cause a space to be put into the output area unless the following tuckword or punctuation would create a double space.

As characters are put into the output area, display lines will be created. Each line will contain not more than 72 characters and spaces and will include only the full words which will fit on the line. When column 72 is reached, the line will be terminated at the first preceeding space. Each display line will contain in addition to the 72 displayable characters, a relative vertical and and absolute horizontal position vector, and a display subroutine return instruction. When the deblocking is finished, the addresses of the first 60 lines of text will be inserted into a display refresh loop. By moving appropriate addresses into or out of this loop, the display "window" may be made to scroll through the text.

A.6 SCAT TERMINAL OPERATIONS

The following operations described in this section will be usable from the display terminal once the SCAT terminal task has been initiated from the PDP-11 control terminal.

A.6.1 Command Level Processing

The SCAT system will be able to operate interactively with the user by means of the function keys associated with the ADDS 500. Each function key will cause an interrupt to the Command Task which will in turn load the modules which are related to that function. The keys will initiate specific operations within three major functions: algorithm development, message processing, and search execution. A breakdown of the function keys will show the functions which are available to user in the SCAT system.

A.6.1.1 Retrieve Algorithm

This key will request an algorithm name as input and will then fetch the named algorithm for execution or edit.

A.6.1.2 Enter Algorithm

This key will blank the screen and initiate the computer assisted algorithm entry routine described below.

A.6.1.3 Edit Algorithm

This key will allow the use of the edit functions described below on the algorithm currently displayed which may have been entered or retrieved.

A.6.1.4 Compile Algorithm

This key will compile the currently displayed algorithm which may have been created, edited, or retrieved. The compilation process is described below in more detail.

A.6.1.5 File Algorithm

The source of the currently displayed search algorithm will be saved. The name must be provided by the user. If the name is an existing algorithm, it will be replaced, otherwise a new entry in the algorithm file is created.

A.6.1.6 Execute Search

The system will request input of search parameters which are the filename(s) to be searched, and options

to be included in the hit list. After these are entered, a search will be performed by applying the algorithm displayed when the execute key is struck to the file)s) named.

While the search is in progress, the hit list items specified will be transferred to a buffer until either the search is complete or the buffer is filled. If the buffer is filled before the search is complete. the search will continue but the hit list will be incomplete. A message giving the total number of hits and the number of hits for which information was recorded will be a part of every hit list so that the user may determine if buffer overflow occured.

The items which are automatically included in each hit list and the optional data which the user can select are:

1. Minimum Information (included by system)

   Message Accession Number
   ADF Sector Address (not displayed)
   Message address within sector (not displayed)
   Total number of hits found and recorded

2. Optional Information (may be selected by user)

   Header Information

      Full header
      Date
      Time
      Source
      Message ID
      Addressee
      Category
      Subcategory

   Full text
   File name where message was found
   Hit mask that indicates which keys caused the hit

A.6.1.7 Display Hit List

This key will display the list of hits found by the most recently executed search. The hit list will always contain (but not display) the sector address and location of each hit and will always display the accession number of each hit. Optionally, the hit list may display any header attribute, the file name in which the message

was found, a hit mask which identifies keys matched in the message, or the full text of the message.

The user may select one or more messages to be displayed for reading, editing, and/or refiling. If only a few hits on short messages are expected, a useful option is to include the text of the message in the hit list so that the user does not need to read the ADF to get the text.

A.6.1.8 Display Message

If a message was selected from the hit list, it can be read directly using the undisplayed location data in the hit list. If this key is used when a hit list is not displayed, an accession number and optionally a file name must be entered. A search will be executed for the accession number.

The message will be displayed and the edit functions may be used on the text of the message if desired. If the total message cannot be displayed on the screen, it may be scrolled.

A.6.1.9 File Message

The FILE MESSAGE key may be used while a message is displayed after being retrieved, created, or edited. There are various options available.

1. Add the edited message to the file containing the original.
2. Replace the original message in the same file.
3. Copy the message to another file.
4. Copy to another file and delete the original.
5. Delete the original message.

A.6.1.10 Collect Messages

The COLLECT key will allow the user to edit and collect portions of the text of several messages into a single message with header and commentary added. The first action in creating such a collection is to create a message header and commentary if desired. Rather than filing this message after its creation, hit the COLLECT key which will put the message into a working file. Then each message from which information is to be copied is called up, all but the desired information is deleted, and the "COLLECT MESSAGE" key is used to add the remaining (undeleted) information

to the working file. Upon completion, "EXIT" may be used to call up the working file for further editing or for filing.

A.6.1.11 Enter Message

The ENTER MESSAGE key will blank the screen and allow for the creation of a new header and message using the edit functions.

A.6.1.12 Display Keys

The DISPLAY KEYS key will allow the user to see the keywords that caused a hit. This function will work only if the user has chosen the hit mask as one of the hit list optional parameters and the message was selected from the hit list.

A.6.1.13 Exit

The EXIT key is used to terminate certain interactive operations such as editing or entry of a message or algorithm.

A.6.1.14 Reset

Reset will allow the user to exit from a process during execution. It will terminate both interactive and non-interactive operations. The files which may have been created up to that point will not be saved. After this function is used there can be no recovery.

A.6.1.15 Help

This key will provide information to assist the operator in the use of the system. The "HELP" key may be pressed at any time. It will save the current contents of the display and the cursor position. Information which may be requested by the analyst will include:

Function currently in control.
Options currently available.
List of names of filed algorithms.
List of format names
List of attributes and coded values for each format
List of file names which may be searched, active, and permanent.
List of system functions.

After viewing the information, the analyst may press "EXIT" to return to the status before he requested the help display, or press "RESET" to abort the current function and return to the command module.

A.6.2 Algorithm Entry

The keystrokes necessary to enter an algorithm are reduced to a minimum by the computer assisted entry routine. This routine is used each time the EDIT ALGORITHM function is used with a blank screen. It will also assist in adding new terms when editing an existing algorithm. The entry routine will also allow the use of the matrix keys to enter frequently used words with a single keystroke.

A.6.2.1 Format Term Entry

Upon entering the algorithm entry routine, the computer will erase the screen and insert the word "format:". The analyst responds by typing a format name followed by a period. After the period is entered, the computer will look up and verify the format name and display the word "header:" on the line below the name.

A.6.2.2 Attribute Name and Compare Operator

If no header terms are desired, the analyst presses the "TEXT" key and the word "header:" will be replaced by "text:". If any header terms are desired, the analyst types an attribute name followed by a tab. The attribute compare operator is entered next by either one of the operator keys or by using character keys. If an operator key is used, the computer will automatically tab to the next field. Compare operators are: "EQUAL", "GREATER THAN", "LESS THAN", and "BETWEEN". Any operator may be preceeded by "NOT".

A.6.2.3 Attribute Value Entry

The value(s) are entered next followed by a period. The period will cause the computer to verify that the attribute name is valid and that the operator and value(s) are permitted with that attribute.

A.6.2.4 Attribute Term Link Entry

The computer will display the link operator "AND" on the line below. Another term may be entered, or the

analyst may modify the link by use of NOT or parentheses. If he types another link operator key (OR, XOR), that operator will replace AND. If he types a left parenthesis, it will appear at the operator position and the operator will be indented. If he types a right parenthesis, it will appear following the previous term and the "AND" will be moved left one tab position.

A.6.2.5 End Header, Start Text

When all header terms have been entered (or immediately after the format name) the analyst presses the "TEXT" key which will cause the computer to replace the link AND with the word "TEXT:" and prepare to accept text terms. Unpaired parentheses in the header terms will be reported at this time. If no header terms were entered, "header:" will be replaced. If no text terms are desired after the header terms, the "EXIT" key may be pressed.

A.6.2.6 Text Term Entry

Each text term is entered as a series of elements separated by commas. An element is either a word (containing no spaces), a phrase (words separated by spaces), or a range (two words separated by the "BETWEEN" operator).

A.6.2.7 Wild Card Characters in Text Elements

A word is a string of adjacent characters terminated by a space or punctuation character. If the word to be searched for may have several endings or possible spelling variations, "don't care" or wildcard characters may be used to construct the keyword for the search. The question mark (?) is used to represent exactly one single don't care character. The crosshatch (#) is used to represent either zero or one character. The asterisk (*) is used to represent any number (zero, one, or many) of don't care characters at the end of a word only.

For example:

Keyword	will match:
launch*	launch, launched, launching, launches, launch-pad, ...
?osmos	kosmos, cosmos, ...
react??	reactor, reacted, ... but not: react, reacting reaction, ...

react##	react, reacts, reacted, reactor, ... but not reaction, reacting.
man*	man, man's, manned, manning, manufacture, manipulate, ...

A.6.2.8 Text Term Link Entry

The computer will display the link "AND" on the line below. "NOT", "OR","XOR", and parentheses may be entered as described in step 3. Additionally, the text portion of the algorithm, the "WITHIN" link may be used. Within must be followed by a proximity specification. This is one or two signed numbers specifying the number of non-tuckwords which may occur between text elements matching the two terms referenced by the within. The computer will automatically insert a bracket in front of the first term referenced by the within link, (which is the first previous term not linked by within) and will follow the second term with a bracket after it is entered. Up to three within links may be nested. The numbers giving the proximity may be plus (to the right) or minus (to the left). One number can be entered with both plus and minus signs. The total width of the proximity limits within nested terms cannot exceed seven.

A.6.2.9 Algorithm Termination

When all terms have been entered, the "EXIT" key is pressed to terminate the algorithm. This will cause the Link Operator following the last term to be replaced with "end". Unbalanced parentheses will be reported. Control returns to the command level.

A.6.3 Search Algorithm Compilation

After an algorithm has been entered or edited, it must be compiled before it can be executed. The compilation process will indicate any errors or warnings to the operator by blinking or otherwise identifying the name, word, or operator which caused the error.

The compiler will accept the search algorithm input by the operator and translate it into an associative processor search program consisting of single valued attribute blocks, multi-valued attribute blocks, and text keyword blocks, link operators, quote field qualifiers, and the header attribute location data.

The compiler may sort or modify the algorithm as input and will display the modified algorithm to show any changes which may have been required.

A.6.3.1 Value and Keyword Validation

As the first step, the compiler will look up each named item (format, attribute, value) and verify that the name is valid. The value names will be encoded. Each text element (word or phrase) will be compared to the tuckword dictionary entries. Tuckwords which follow non-tuckwords in phrases will be encoded. Note that tuckwords may neither begin a phrase nor be a single word element.

A.6.3.2 Keyword Sort

The compiler will sort the text keywords and the attribute values into the proper order for the search program. This sort will insure that single valued attributes preceed all multi-valued attributes and that any keywords which appear in quote fields are within the first eight text keywords. This may require inserting additional parentheses and duplicating certain keywords within the groups formed by the parentheses and/or modifying the link operators in order to preserve the logical relationships of the original algorithm.

The sort will identify each attribute value and text keyword with a number from 1 to 32 which can be used to relate the keywords to the hit mask resulting from a search.

The keywords, attribute values, parentheses, and link operators in the sorted search algorithm will be examined to determine if they can be blocked into a search program. This will require blocking the search algorithm so that the following limits are not exceeded.

1. There may be no more than four program blocks. A block may contain up to eight text keywords, one value for each of up to eight single valued attributes, or up to eight values each for up eight multi-valued attributes. Each block may contain only one of the above types.

2. Each block must have its elements linked to the elements of other blocks by a single operator.

3. The first text block must contain all keywords which appear in phrase elements and/or in terms linked by the within operator.

A.6.3.3 Quote Field Pattern Synthesis

The keywords used in phrases or in terms linked by within operators will be examined to see which combinations of words can be permitted in the text to match the search algorithm specification. The result of this will be the quote field bit mask for the search program.

A.6.3.4 Header Attribute Location

Location data will be retrieved from the format definition table for each attribute. This data is also inserted into the search program.

A.6.3.5 Text blocking

All text keywords will be separated into words and phrases which will be blocked the same as input messages are blocked.

A.6.3.6 Error Indications

Errors will be reported by blinking the offending element and displaying an error description.

A.6.4 Message and Algorithm Edit

The edit module will be used for keyboard editing of both message text and search algorithms. When editing the functions below will be available. Upon completion, press the EXIT key to signify completion of the edit. The edited material may be filed either as a new item or as a replacement for a previous version.

The matrix keys may be used while editing both for cursor control and for entry of frequently used words.

A.6.4.1 Cursor Control

The cursor control module will allow the operator to move a displayed cursor to any position in the displayed data (up, down, right, left, new line, tab) except the header of a message.

A.6.4.2 Character Insert

Character Insert will permit individual characters

to be inserted on a line. Characters to the right of the character entered will be moved to the right with a new line being inserted if non-blank data is at the end of the line.

A.6.4.3 Line Insert

Line Insert will insert a blank line below the line containing the cursor.

A.6.4.5 Line Delete

Line Delete will delete the line containing the cursor.

A.6.4.6 Character Overwrite

In normal mode, characters will overwrite the current data. This is usually used to enter new data on a blank line.

A.6.4.7 Line Join

Join will join two adjacent lines and reduce multiple spaces between words to single spaces.

A.6.4.8 Line Break

Break will split a line and left justify the right most portion of the text on a new line inserted below.

A.6.4.9 Paging

The display can show about 60 lines of 72 characters. If a message is longer than this, the operator can scroll the text past the "display window" to view or edit the entire message.

A.6.5 Matrix Keys

The key matrix to the right of the main keyboard will provide for cursor control and also several frequently used words which could be entered by typing out the letters of the word, but by using the matrix key to enter the function, the entire word is entered with one keystroke and in most cases, the field terminator (carriage return or tab) is assumed also.

In addition to up, down, right, and left cursor control, the following words are used:

not.....NOT operator for attribute compare or term link.

and.....AND link operator.

or .....OR link operator.

xor.....EXCLUSIVE OR (XOR) link operator.

between.....BETWEEN text or attribute compare operator.

less than....LESS THAN attribute compare operator.

grtr than....GREATER THAN attribute compare operator.

equal.....EQUAL attribute compare operator.

within.....WITHIN link operator.

open paren...Left parenthesis.

close paren..Right parenthesis.

A.7.0 RECORD FORMAT DEFINITIONS

The format of each type of record stored on the ADF will be described in a format definition table. The user may add additional format tables to the system after delivery. The system as delivered will provide for two ADF record formats, message and algorithm. There will be only one batch input format, message.

A.7.1 Message Format

Data records in the initial system will be teletype messages. The format of a message shall be defined for three states: 1. input or TTY format, 2. display or ADDS format, and 3. blocked or ADF format.

A.7.1.1 Header Input Format

Each message shall be stored in the input file with a header in the following format. If any item is blank because the data is unknown or omitted, a null must follow the tab or carriage return.

control data character item — contents of field or control char. code.

SØH		octal 201
	source	three to eight ASCII characters, must be a valid source name in format definition table
TAB		octal 214
	day	two ASCII numeric digits
	month	three ASCII alphabetic characters
	year	two ASCII numeric digits
TAB		octal 412
	time	four ASCII numeric digits, 0000-2359
SPACE		octal 240
	time zone	three spaces or three alphabetic characters
TAB		octal 214
	message ID	one to six numeric digits
CR		octal 215
LF		octal 212
	addressee(s)	Up to eight characters each, separated by a comma and space. There may be up to 16 addressees. Each must be a valid addressee name in the format definition table.
CR		octal 215
LF		octal 212
	category code	Up to eight characters each, separated by a comma and space. There may be up to 16 category codes. Each must be a valid category name in the format definition table.
CR		octal 215
LF		octal 212
	subcategory	Up to eight characters each, separated by a comma and space. Each must be a valid sub-category code in the format definition table.
	code	
CR		octal 215
LF		octal 212

A.7.1.2 Text Input Format

All input records which have text shall use the following format for the text. The header shall be

followed immediately by the message text. Text shall start with an STX character, octal 202, and terminate with an ETX character, octal 203. The text between may be any of the 64 ASCII characters, octal 240 to 337, and also CR, LF, & TAB. The text may contain as few as two characters, STX - ETX, or as many characters as will fill an ADF sector when blocked with header, about 12K bytes.

Carriage return and/or line feed characters are required only when a word is to be put in a specific position, as for the first line of a paragraph or in tabular data. Tab will position text to the next higher column in the tab table which will be: 08, 16, 32, 48, 64. Any sequence or occurrance of carriage return and/or line feed will be assumed to have a minimum of one line feed and exactly one carriage return. The system will automatically break each line at the last space before character 72 unless character 73 is a space. Input text must not contain strings of more than 72 characters without spaces.

A.7.1.3 ADF Message Format

The messages will be blocked as described in 5.4 before storage on the ADF.

A.7.1.4 Message display format

Header deblocking will require looking up each attribute value in the format definition table and inserting the ASCII characters found there into the fixed length areas of a header display block.

Text deblocking will be performed on a byte by byte basis. Each byte will be examined and the appropriate data will be put into the output area. Character bytes will be moved directly to the output area. Punctuation bytes will be translated to the indicated symbol(s). Tuckword bytes will be translated to the encoded tuckword, preceeded and followed by a space except where a punctuation byte following or preceeding would create a double space. If used, the word compression bytes would be translated into a string of characters. Repeated byte groups will be expanded.

As characters are put into the output area, display lines will be created. Each line will contain not more than 72 characters and spaces and will include only the full words which will fit on the line. When column 73

is reached, the line will be terminated at the first preceeding space. Each display line will contain in addition to the 72 displayable characters, a relative vertical and an absolute horizontal position vector, and a display controller jump or branch instruction. When the deblocking is finished, the first 60 lines of text will be inserted into a display refresh loop. By changing appropriate addresses of branch instructions, the display "window" may be made to scroll through the text.

A.7.2 Algorithm Formats

A.7.2.1 Algorithm Source Format

The source format for search algorithms shall be similar to message display format for text except that extra spaces and tabs shall be eliminated. That is, each line shall be preceeded by a position vector and the characters will be arranged for display. In algorithm source, the position vectors will identify the position of the first displayable character on the line. While editing, there may be spaces in front of the first displayable character, but before compilation or storage, all leading spaces or tabs will be replaced by equivalent position vectors.

A.7.2.2 Algorithm Object Format

When an algorithm is compiled, a reformatted source and an object version will result. The object algorithm is a block of up to 4K bytes of data in exactly the format which is required by the associative processor. The program or associative processor search algorithm when encoded for processing will have the following:

One general information slice containing the message format to be searched, the program length, etc.

One block mask slice containing the start and end locations of each program block.

32 slices of link bit mask, giving the patterns of the 32 bit hit mask which will result in a message hit.

One optional slice of quote mask specifying the order in which the keywords of the first text block must appear to get a quote hit.

Zero to four slices of header attribute location data defining which attribute keys are to be compared against which attributes in the header.

Zero to four blocks of attribute and text keys. Each block will be a variable number of slices.

The header block will have a number of slices of one-on-one keys and a number of slices of keys for multi-valued attributes.

Each text block will have up to eight text keywords and the compare operator for each character.

A.7.3 Graphic Data Format

The SCAT system has the capability to store records containing graphic display information (such as maps or line drawings) with a header and/or text. Searches may be done on the non-graphic data only. When retrieved, the graphic data will be displayed without translation. The other data will be shown in an unused portion of the display.

A.7.4 User Provided

The user may provide format definition tables to describe any record format consisting of header only, text only, header and graphic data, or text and graphic data. He must also provide the appropriate routines to input and/or create and edit these records. The search algorithm compiler will handle searches for the new records if the format name has been included in the list of valid formats and the format definition table has been provided.

A.8.0 OPTIONAL SOFTWARE MODULES

A.8.1 ADF Directory File Recovery

If the ADF directory is lost or incorrect, the entire contents of the ADF will be unreadable unless the directory can be restored. Operating system errors like being unable to open the file, read or write the file, or having the System Directory destroyed would make the Directory invalid. If this occurred, all addresses, dates and files on the CDC disk might be valid but accessing the ADF for reads, writes, updates, etc., could not be accomplished. Therefore, a utility to restore the directory is needed to keep the integrity of the Data Base.

In order to restore the directory, each sector on the CDC disk will have a header record containing the file name the sector belongs to, the physical sector number, last location used in the sector and any other pertinent information. The recovery program can locate where each file within the active file is, how much reserve space is left in each file, how many active day files there are, and how large each file (whether active or inactive) is.

A.8.2 Data Base Compacting

Compacting of a file will maximize the storage of messages on the ADF disk. File compaction could be done at the end of each day or at the option of the operators. Compacting a file involves shifting messages in order to fill up the "holes" left within the files by deletion or editing of messages.

A.8.3 Data Base File Management

The Data Base File Management module will allow user to modify the files contained within the Data Base. This will include the ability to create, delete, expand, insert and contract files within the Data Base. Judicious use of this utility can enhance searching by setting up related files sequentially, or allow the analyst to expand files that have reached capacity, or delete files no longer needed, or to create files to save information as a new category.

A.8.4 Hit File Creation

The analyst may have a large amount of messages found from the execution of a search algorithm. This information could be saved in a new file for later processing. The search will not have to be done again and editing, deletion, etc., on this file can be done in a more organized fashion.

A.8.5 Active File Recovery

Recovery of the contents of the active file is not envisioned as part of the initial system, but its function will be described. If the data stored in the Active File for any given day(s) was found incorrect because of some system malfunction, there is a possibility to restore the data relative to a given day if the original data has been preserved.

In the initial system as proposed, the only recovery possible is by saving the RK-05 disk that contains the data associated with that days active file. Restoration of this data is incomplete because all editing and commentary done since that day will be destroyed. The data restored will be the original data input to the Data Base.

If a more up to date restoration is required, then a journaltape or a back up data file on the system disk would have to be maintained. This type of recovery is a major software effort and is not being considered for implementation.

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